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Enhancing Communication Technologies with Advanced Optimization of 5 GHz Low Noise Amplifiers

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Abstract

Radio frequency integrated circuits (RFICs) are widely used in wireless technology systems. Low-noise amplifiers, especially in the 5 GHz frequency range, are vital parts of contemporary wireless communication systems. Research on 5 GHz low-noise amplifiers aims to improve the performance of these amplifiers by addressing issues related to noise, gain, and power efficiency. Low-noise amplifiers are used in many different applications and are essential for developing more effective, efficient, and balanced wireless communication systems. The paper presents a wideband low-noise amplifier (LNA) implemented in a 5 GHz (Low-Noise Amplifier) for 5G Wi-Fi applications. It is driven by a 1.8 V supply. To increase the voltage gain and reduce the power consumption, the circuit has a common source layout and is optimized to reduce the noise figure. Single-stage common source decomposition and inductive source decomposition techniques are also used to match the circuit with the source impedance. Genetic algorithm is also used to optimize the circuit operation. The genetic algorithm has been shown to significantly reduce the noise in the low-noise amplifier circuit, which greatly improves the signal quality. The algorithm has increased the gain of the circuit, making it more sensitive to signals and enhancing its ability to process diverse signals. The proposed LNA showed a total current of 2 mA and a minimum noise figure of 1.107 dB with a high voltage gain of 21.86 dB and a power consumption of 3.6 mW. I expect the proposed LNA to be suitable for 5G Wi-Fi applications in the GHz band.

Keywords
Noise Figure, 5G Wi-Fi Applications, Power Gain, CMOS Technology, Optimization, Active Inductor.

I. INTRODUCTION

Radio frequency integrated circuits (RFICs) are the brains of advanced wireless communications systems. These analog circuits, which have a reputation for being highly efficient, operate at 5 GHz operating frequencies. The first component in a series of radio receiver components, one of the problems with these circuits is that they can receive the signals that are not suitable for display, so a low-noise amplifier (LNA) amplifies weak signals from antennas with the lowest possible noise level. When designing a low-noise amplifier (LNA), it is essential to find a balance between power consumption and noise coefficient, to create an integrated design that serves different applications [1–3]. When boosting wireless signals, may encounter additional noise, which prevents us from getting the most out of the signal. Achieving a suitable circuit design is critical, but it is even more important to find a balance between the additional noise and the gain get. Perhaps the greatest way to overcome technical challenges and produce and balance circuit performance is through optimization. Designing a low-noise amplifier that can effectively balance these parameters is a complex engineering challenge. Traditional design methods often fail to achieve optimal performance. The one is optimization techniques, such as genetic algorithms. By mimicking the natural process of evolution, genetic algorithms can efficiently explore a wide design space and identify nearly optimal solutions. They are capable of solving and optimizing complex nonlinear systems [4, 5]. The field of low-noise amplifiers has seen significant developments

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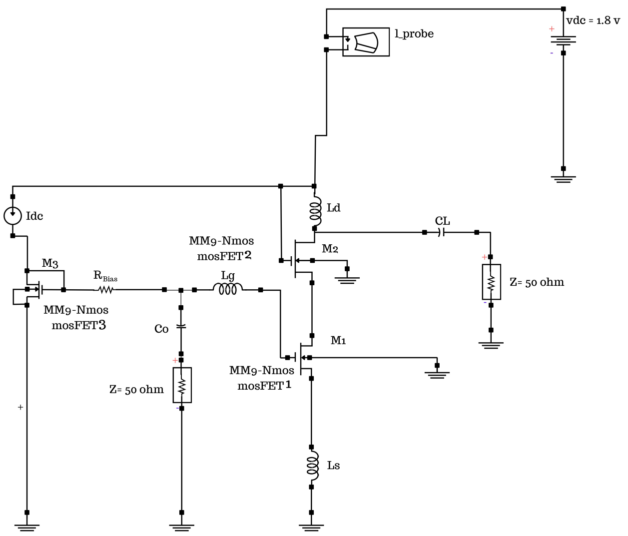

Fig. 1. Single-Ended LNA

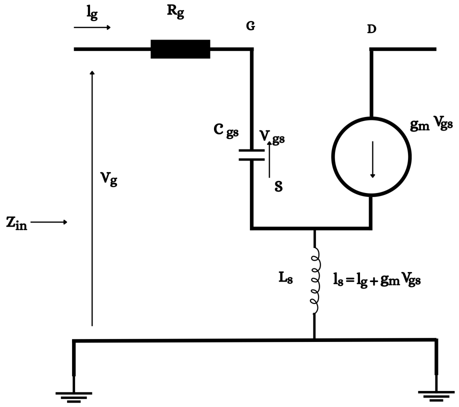

Fig. 2. New Equivalent Model of MOSFET with Source De Generation Added

in recent years, with researchers focusing on improving the performance of these amplifiers by developing new transistors, using innovative materials, and applying advanced manufacturing techniques. These developments have greatly enhanced the efficiency of these amplifiers and reduced the noise level, expanding their range of applications in areas such as wireless communications and sensitive sensors. Therefore, the low-noise amplifier application model presented in the study was created using 180 nm CMOS technology and circuit simulation using ADS software. As can be seen in Fig. 1, two approaches—analytical tools and optimization tools applied and compared to demonstrate the value of optimization in LNA design. The genetic algorithm is used in MATLAB to address complex optimization problems because it uses the principles of biological evolution to arrive at nearly optimal solutions. For the optimization features in MATLAB used. In addition, the approach can be easily used and updated due to the powerful MATLAB environment, giving researchers and engineers a valuable tool to improve their models and designs [6].

II. LOW NOISE AMPLIFIER DESIGN

A. *Basic Low Noise Amplifier Realization and Topologies:*

The paper examines a number of topological approaches to low-noise signal amplifiers; each approach has advantages and disadvantages of its own, offering analogy circuit designers a range of options to meet application needs. Basic topologies include the differential low-noise amplifier and the single-ended low-noise amplifier [7]. Because CMOS technology can be produced as a single-piece integrated circuit and is easy to operate, it is a desirable method for creating low noise amplifiers. The design of a single-end narrowband, low-power, low-voltage, low-noise amplifier involves a number of fundamental investigations, as illustrated in Fig. 2. These include resistive-end common sources, common gates, chain-link common source feedback, common source magnetic loading, and cascade source loading [8].

B. *Single-Ended LNA design:*

The system is designed (Single-Ended) such that the real part of the input resistance can be precisely adjusted by choosing the appropriate inductance value. To enhance isolation between the tuned input and output, a second transistor, M2, is used in a cascade configuration. This arrangement helps reduce mutual influence between tuned circuits. Transistors (M1) and (M3), arranged to form a current mirror, are skillfully used in the design of the bias system. (M3) was specially chosen to ensure minimum power consumption of the bias function. To increase the efficiency of power transfer to the output, resonance with the external load is generated through the use of an inductive coil called (Ld). The ability of an LNA to amplify signals with minimal additional noise and with the best possible power consumption depends largely on this precise coordination of parts and their interactions. In the schematic diagram shown in Fig. 1, a single-ended low-noise amplifier (LNA) is presented, in which an inductive coil known as Ls is strategically connected at the source terminal of the transistor, a technique known as inductive source damping. The arrangement is used to improve the noise and stability characteristics of the amplifier [9].

III. SYSTEM AND DESIGN

A. Mathematical Analysis of Single Ended LNA at 5 GHz with 180 nm Technology:

To ensure compliance with critical parameter values for performance specifications, accurate values for key parameters must be defined and applied [10]. Within the design process, the best dimensions for MOSFETs labeled W1, W2, and W3 are sought. This also includes determining the inductance values for the degenerative inductance (LS), gate inductance (Lg), and drain inductance (Ld). In addition, the design includes choosing the appropriate interconnect capacitance values, namely the load capacitance (C2) and the input capacitance (C0), as well as setting the correct bias current (Id), while ensuring consistency between the values of the circuit elements. The simplified small signal equivalent circuit is also explained in a specific way. The calculated input impedance for a single-ended LNA amplifier has been documented in the technical references [11].

$$Z_{in} = R_g + (\frac{gm}{C_{gs1}})L_s + j(wL_s - \frac{1}{wC_{gs1}}) \tag{1}$$

Equation (1) can be formulated as follows [11]:

$$Z_{in} = R_g + R_a + j(xL_s - X_{cgs1}) \tag{2}$$

Where

$$R_a = (\frac{gm1}{cgs1}L_s) \tag{3}$$

The means that the impedance without feedback from the MOSFET will be:

$$Z_{in} = R_g - jx_{cgs1} \rightarrow Z_{in} = -j(X_{cgs1}) \tag{4}$$

When series feedback is added, a term is added to the original input impedance. Another inductive coil is added with the gate Lg in sequence chosen to resonate with the capacitor Cgs. The value of Lg was chosen to cancel out the effect of Cgs and thus achieve exactly. $Z_{in} = (\frac{gm1}{cgs1})L_s; Z_{in} = 50\Omega$ In most LNA designs, the Id value is chosen, and then the gm and Cgs values are obtained to provide the required input impedance Rin. Considering the use of a 180nm process, for an operating frequency of 5 GHz and based on the given process parameters [11, 12].

Step1. The width of the MOSFET 1 (M1) MOSFET (M2) transistor device is determined according to reference [13].

$$W_1 = \frac{3}{2 \times C_{ox} \times L_1 \times Q_{OPT} \times w_O \times R} = 100\mu m \tag{5}$$

Step2. The Gate to source capacitor Cgs is calculated as:

$$Cgs = \frac{2}{3} \times C_{ox} \times W_1 \times L_1 = 0.0985\text{PF} \tag{6}$$

Step3. Trans-conductance (g_{m1}) of MOSFET1 (M1) is given as [14]:

$$g_{m1} = \sqrt{2 \times \mu_n \times C_{OX} \times \frac{w}{L} \times I_d} = 32.72\text{m} \tag{7}$$

Step4. Therefore, the transistor unity gain frequency W_T is:

$$W_T = \frac{g_m}{C_{gs}} = 332.27\text{Grps} \tag{8}$$

Step5. The minimum noise figure is given as [14]:

$$NF = (1 + 1.62 \times \frac{W_O}{W_T}) = 1.153 \tag{9}$$

Step6. Then the voltage gain can be determined as [15]:

$$A_V = 20log(\frac{1}{C_{gs} \times W_O \times 50}) = 16.213 \tag{10}$$

Step7. The values of L_S , L_g , and L_d are obtained as follows:

$$L_S = \frac{R_S}{W_T} = 0.15n\text{H} \tag{11}$$

Where R_S is the input resistance 50 Ω

$$L_g = \frac{1}{W_O^2 \times C_{gs}} - L_s = 10.13n\text{H} \tag{12}$$

$$L_d = \frac{1}{W_O^2 \times C_{gs}} = 3.38n\text{H} \text{Where CL=0.3 pF} \tag{13}$$

Step8. The power dissipation is then calculated to be:

$$P_D = V_{DD} \times I_d = 7.2\text{mW} \tag{14}$$

Where I_d is the current $4m$A

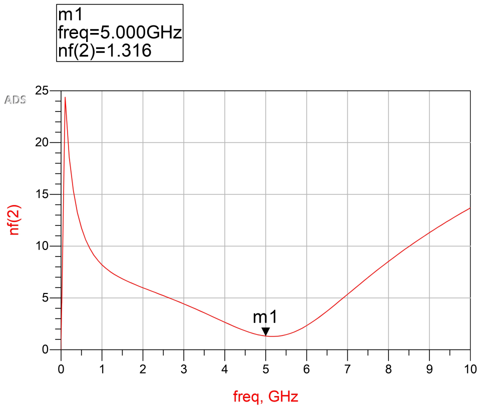

Fig. 3. Analytical Results for Noise Figure of Single-Ended LNA at 5 GHz

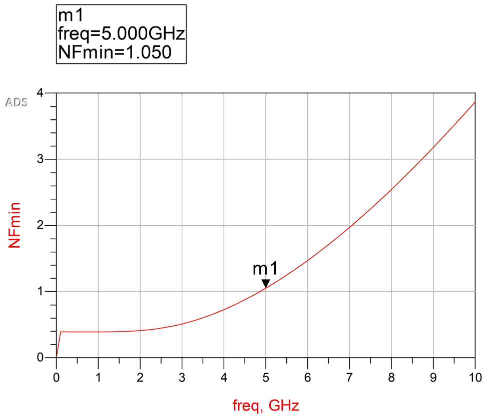

Fig. 4. Analytical Results for Minimum noise figure of Single-Ended LNA at 5 GHz

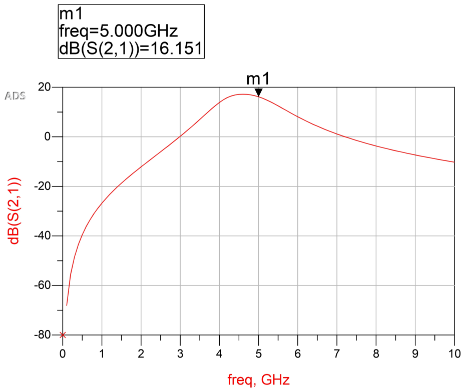

Fig. 5. Analytical Results for Power Gain of Single-Ended LNA at 5 GHz

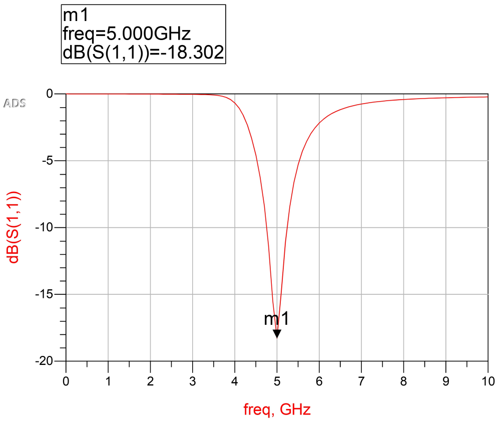

Fig. 6. Analytical Results for Input Return Loss S11 of Single-Ended LNA at 5 GHz

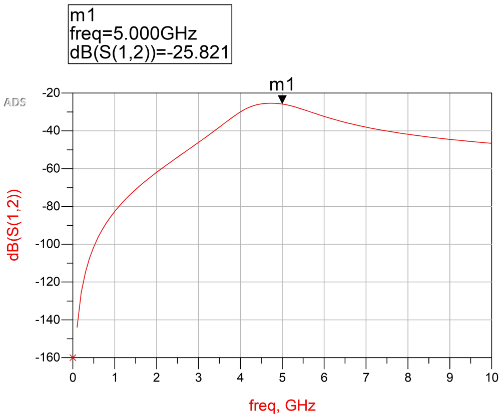

Fig. 7. Analytical Results for Revers isolation of Single-Ended LNA at 5 GHz

Mathematical analysis was performed to determine component values for the low noise amplifier (LNA), and these to be successfully simulated using Advanced Design System (ADS) RF simulation software. The single-ended amplifier circuit, based on 180nm CMOS MM_9 parameters, is powered by a 1.8 V power supply and consumes 7.2mW.

After conducting mathematical simulation, the extracted values as obtained NF = 1.316, NF min=1.05, gain=16.151 , dB(S(1,1)) = -18.302 and dB(S(1,2))=-25.821 as in Figure 3, Figure 4, Figure 5, Figure 6 , Figure 7.

B. Optimization Results for Single Ended LNA at 5 GHz:

After analysing the results obtained through mathematical laws, all of notice that there is no sufficient balance between the results and the method could not meet the requirements of the applications work satisfactorily on satisfactorily, so it became necessary to work on the genetic algorithm to achieve

TABLE I. DESIGN VARIABLES AND CONSTRAINTS LIMIT USING MOGA.

Variable's name	Constraints values
I_d	1 to 7 m A
W_1	10 to 400 μ m

the required balance and improve the results by providing less noise and greater gain through which the signals can be dealt with and less power consumption. To achieve an ideal design for nanometer-sized MOSFET transistors, it is necessary to rely on genetic optimization algorithms. Due to the complexity of the mathematical models for these relationships, manually determining the values of the optimal design variables is a difficult and perhaps impossible task. Optimization algorithms help overcome these complexities and reduce the time required to reach the optimal values [16]. In radio frequency (RF) circuits, there are many criteria that must be taken into account, and these criteria are often conflicting. Designers must find a balance between different objectives such as profitability, power consumption, noise factor (NF), and others. The MOGA algorithm is preferred in the MATLAB simulation program over other algorithms due to its simplicity, high optimization efficiency, and balance between the required objectives the technique has shown good results in solving complex multi-objective optimization problems, and it was able to discover different solutions to the Pareto front with little computational effort [17, 18]. Figure 8 shows the steps of the procedure for the MOGA toolbox optimization method using MATLAB.

IV. DESIGN OBJECTIVES AND CONSTRAINT OPTIMIZATIONS OF LNA INDUCTIVE SOURCE DEGENERATION

In a genetic algorithm, chromosomes consist of a pair of real numeric values that represent design variables. The two basic elements on which the design is built are (Id and width W1), and the constraints associated with these variables are specified in Table 1.

On the other hand, as indicated in Tables (2) and (3), respectively, (L_S, L_g, and Cgs) are utilized as nonlinear constraint functions to achieve minimization for power maximizing gain, minimizing consumption and noise figure, and fulfilling the required performance criteria. Stated differently, the L_S, L_g, and Cgs functions help guide the evolutionary algorithm to choose the best low-noise amplifier design while ensuring that all requirements are met. This includes taking into account the circuit's gain, power consumption, and noise ratio.

The low-noise amplifier's performance requirements are used in the MATLAB MOGA optimization toolbox. While some of these parameters served as limitations, others taken

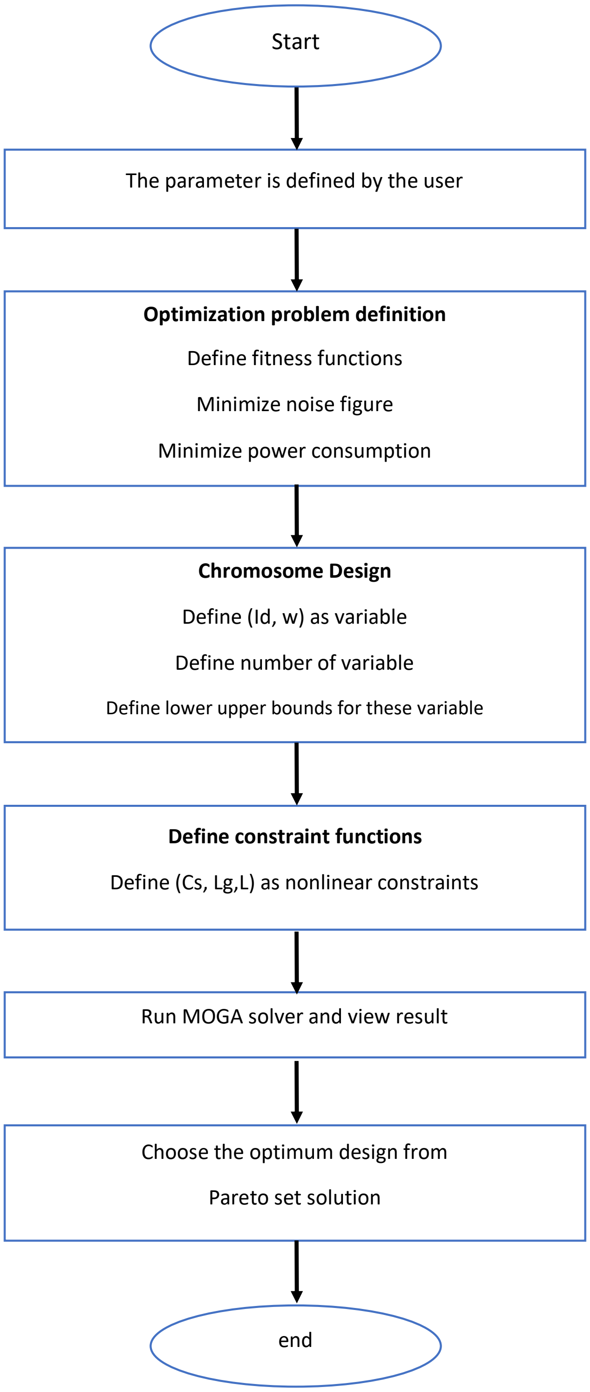

Fig. 8. Flowchart of Genetic Algorithm Procedure Based on MATLAB

TABLE II. CONSTRAINTS LIMIT USING MOGA.

Parameter	Constraints values
$C_{g}s$	0.05 to 5 pF
L_S	0.05 to 3 n H
L_g	1 to 80 n H

TABLE III. LNA Specifications Design Target for 0.18 μ m CMOS Process.

Parameter	value
Frequency (GHz)	5
Supply Voltage(V)	1.8
S_{11} (dB)	$<$ -10
S_{21} (dB)	$>$ 12
Noise Figure (dB)	$<$ 2
Power consumption (mW)	$<$ 8
Source/load Impedance (Ω)	50

into consideration while creating the suggested fitness functions. A summary of these requirements can be found in Table 4.

TABLE IV. DESIGN CONSTRAINTS AND SPECIFICATIONS FOR LOW NOISE AMPLIFIER.

Specifications / Constraints	**Type**	**Equation**
Gain	Fitness Function	10
Noise Figure	Fitness Function	9
Power Dissipation	Fitness Function	14
Gate to Cource Capacitor C_{gs}	Constraint	6
L_S Degeneration Inductor	Constraint	11
L_g Inductance at The Gate	Constraint	12

Once the algorithm is executed, it generates a series of optimal design process solutions. The WSM method, the simplest method, is used to compare these alternatives. Because the approach takes into account the assumption of additive benefit, I can say that the sum of all products equals the total value of all alternatives. When comparing criteria that use the same unit ranges, the WSM method performs well. As shown in Table 5.

TABLE V. OPTIMAL VARIABLES VALUE OF PROPOSED LNA.

Components	Optimization method
Width $W_1\,(\mu$m)	50.24
$I_d\,(m$A)	2.0004
$C_{g}s$ (pF)	0.0493
$L_g\,(n$H)	20.5
$L_S\,(n$H)	0.15
Power consumption (mW)	3.6

V. SIMULATION OPTIMIZATION RESULTS FOR SINGLE ENDED LNA AT 5 GHZ

When the element values obtained via the Genetic Algorithm (GA) are applied, the simulation will be performed and improved results will be obtained.

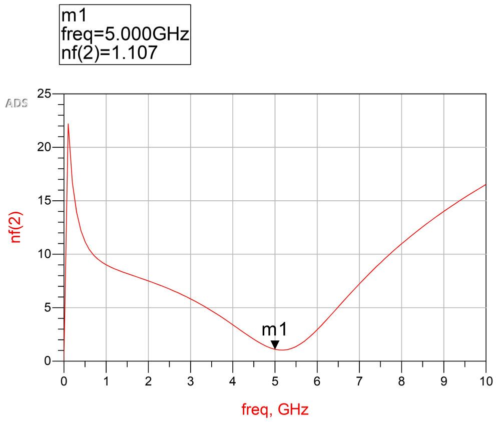

Fig. 9. Optimization Results for Noise Figure of Single-Ended LNA at 5 GHz

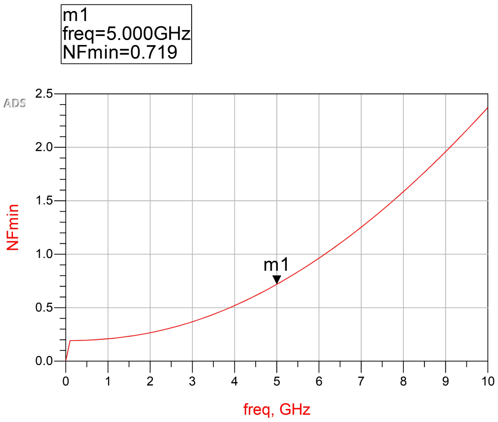

Fig. 10. Optimization Results for Minimum noise figure of Single-Ended LNA at 5 GHz

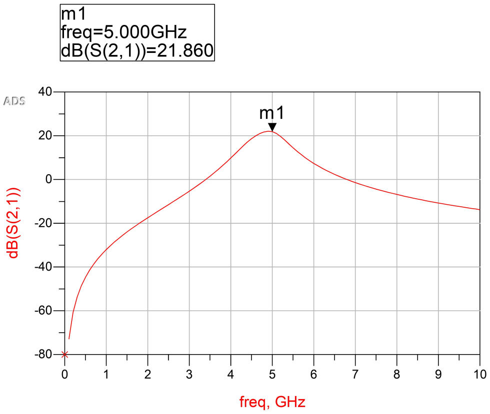

Fig. 11. Optimization Results for Power Gain of Single-Ended LNA at 5 GHz

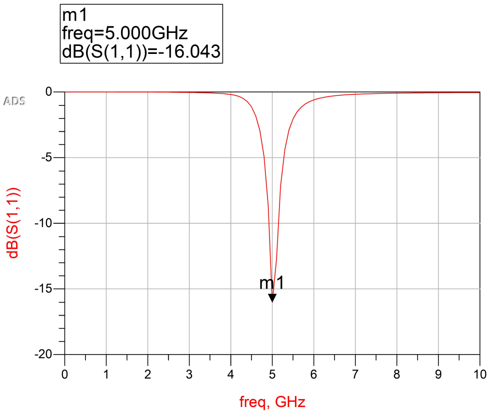

Fig. 12. Optimization Results for Input Return Loss S_{11} of Single-Ended LNA at 5 GHz

The current ad simulator incorporates a MATLAB-implemented optimization method to control the creative process. The algorithm seeks to accomplish several objectives, such as lowering noise level and power usage. it optimization framework additionally incorporates other design standards and criteria as constraints. A comparison of the simulation's optimization strategy and a conventional analytical method—which is based on the design equations [5] specifically at a frequency of 5 GHz. The data suggests that the optimization method significantly enhances performance.

VI. COMPARISON BETWEEN THE OPTIMIZATION TECHNIQUE OF ADS AND OTHER EXISTING LITERATURE

The optimization was compared with other analytical methods [11, 19, 20]. Shown in Table 6. It can be seen that the improvement in design using the optimization compared to the references was obtained [11, 20]. From the comparison in Table 6 shown, the proposed 180nm single-ended LNA (inductive source decomposition as a code), has a low noise figure (NF), low power consumption and high-power gain compared to [11, 20] LNA.

When compared with [19], notice a significant improvement in the noise value but with a gain less than [19] but the essential superiority with all those compared is the great balance between all the results stated in the research paper with good results recorded in all values that fit well with the previously mentioned applications.

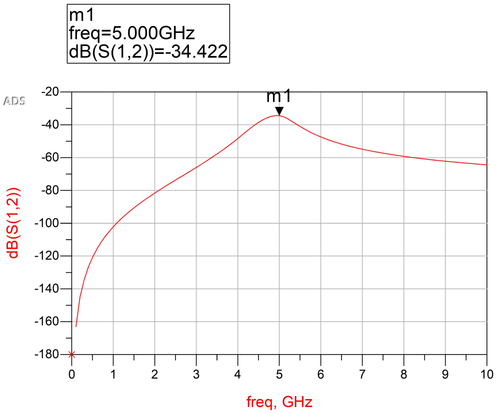

Fig. 13. Optimization Results for Revers isolation of Single-Ended LNA at 5 GHz

VII. CONCLUSIONS

The main contribution of the manuscript how to improve the design of a 5 GHz low-noise signal amplifier by utilizing the optimization tools that are available in the MATLAB simulator. In order to achieve the lowest feasible noise coefficient and power consumption, an inductive source degradation technique was employed. The study and realization of the design specifications was done using an ADS RF simulator that was built using optimization methods that originated from MATLAB algorithms. In the paper, alternative existing methodologies are compared with an existing analytical method. The outcomes demonstrated that utilizing optimization technology reduced both the noise level and energy usage.

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TABLE VI. COMPARISON BETWEEN THE RESULTS OF PROPOSED WORK AND OTHER DESIGN TECHNIQUES [11], [19] AND [20] OF LNA.

Parameters	[11]	[19]	[20]	Proposed Work
Technology	0.18μ m	0.18μ m	0.18μ m	0.18μ m
Supply Voltage	1.8 V	1.8 V	1.8 V	1.8 V
Frequency (GHz)	5	5	5	5
Noise Figure (dB)	1.330	3.2509	3.7	1.107
NF_{min}	1.074	1.2215	NR	0.719
S_{21} dB	20.443	41.355	19.228	-21.86
S_{12} dB	-24.25	10.436	-19.123	-34.422
S_{11} dB	-12.79	-12.44	-14.313	-16.04
$W_{M1}, W_{M2} (\mu \text{m})$	69.128	140	84.75	50.24
$W_{M3} (\mu \text{m})$	6.91	28	74	5.0
Power Consumption(dB)	-27.44	-49.57	0.48	-24.43

Nomenclature	
LNA	Low Noise Amplifier
C_{ox}	Capacitance Per Unit Area of the Gate Oxide
R_g	Cate Resistance
G_{m1}	Device Transconductance for MOSFET
C_{gs}	Cate-source Capacitance
W_T	Unite Gain Frequency of the Mos
NF	Noise Figure
AD_s	Advance Design System
Δf	Noise Cut-off Frequency
$MOGA$	Multi-Objective Genetic Algorithm
S_{21}	Forward-voltage Gain
S_{21}	Input Reflection Coefficient
CS	Common-Source
C_s	Capacitor Source
GA	Genetic Algorithm
$WLAN$	Wireless Local Area Network
WSM	Weighted Sum Method
$TSMC$	Taiwan Semiconductor Manufacturing
RF	Radio Frequency
W	Width of MOSFET
WL	Reactance of Inductance
L	Channel Length
Ld	Drain Inductance

CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

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