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Slantlet Transform-Based ECG Classification System with Efficient Design and Implementation

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Abstract
Since cardiac conditions are among the most fatal illnesses in the medical community, ECG classification systems are crucial for understanding and diagnosing patients' health conditions. Numerous techniques for ECG feature extraction and classification algorithms are developed by researchers. This paper presents a method for accurately classifying ECG illnesses based on the 3-scale Slantlet transform (SLT) and artificial neural network (ANN). The ability of the SLT filters to decompose the ECG signal at various resolutions led to excellent classification. As a new realization, all coefficients of the modified designed SLT filters are expressed by the sum-of-power-of-two (SOPOT) approach to reduce the complexity. It is noteworthy that the average and maximum deviation error values between the responses of original and modified filters are very small. Hardwarely, the new realization leads to a less complex implementation for the designed SLT filters on FPGA kit using the Xilinx System Generator for DSP with very small errors between output resposes of the original and modified filters. FPGA results show that the system is designed using a best-selected wordlength method. The proposed classification system is capable of distinguishing the ECG normal case and other four different diseases with a high overall accuracy of 98.50 %.

Keywords
Electrocardiogram Signal (ECG), Slantlet Transform (SLT), Artificial Neural Network (ANN), SOPOT, Xilinx System Generator (XSG), FPGA.

I. Introduction

Electrocardiogram (ECG) represents the electrical activity of the heart. Physicians use ECG signal shapes to predict various cardiovascular diseases and prescribe their appropriate treatments. Therefore, the diagnosis of ECG signals has a vital role in patient's health, in the early detection of arrhythmia types and is significant in picking the suitable treatment for patients [1, 2, 3].

Essentially, for non-stationary signals like ECG signals, it is known that the discrete wavelet transform (DWT) is suitably used for feature extraction. In other words, DWT is an effective tool for many applications requiring multiresolution analysis. In addition to its facility of time-discrimination, DWT provides variable-width windows which can be easily chosen as narrow for high frequency discrimination and wide for low frequency discrimination. The DWT filter bank is usually carried out by iteration. But, for a fixed number of zero moments, this does not yield a discrete-time basis that is optimal with respect to time-localization. In 1999, Selesnick proposed a bank of filters known as Slantlet transform (SLT) which can provide better signal compression and better time localization compared to the discrete wavelet transform (DWT) and to discrete cosine transform (DCT), it is orthogo-

nal with two zero moments and retains the basic characteristic of the filter bank such as octave band [4, 5, 6]. SLT is a recent-good multiresolution tool which is appropriate for a piecewise linear data. Completely like the DWT filters, the SLT filters are orthogonal and can offer multiresolution decomposition. The structure of Slantlet filters is implemented as a set of parallel filters with different lengths, whereas the structure of DWT filters is implemented based on filter bank iteration as a tree structure [7, 8].

In this work, ECG classification system is introduced based on three-scale SLT filters with a less-complex realization for features extraction of ECG signals. The SLT filters are designed based on the idea of the multiplier-less representation which leads to a farther reduction in the number of mathematical operations. All SLT coefficients can be represented based on the sum-of-power-of-two (SOPOT) method as multiplier-less realization and implementation. In hardware, this leads to easy implementation on FPGA with less chip area and high speed. The artificial neural network will be used as classifier system to diagnosis heart diseases.

Besides this introduction, Section II presents an overview of the SLT filter banks, including the SLT structure and the filters length compared with the DWT. In section III, the 3-scale SLT filters with less-complexity are considered depending on the sum-of-powers-of-two with minimum error values in the magnitude/phase responses. In the section IV, the implementations and results of FPGA are shown. An ECG classification system is introduced in section V. Finally, Section VI concludes this paper.

II. Slantlet Filter-Banks

In 1999, Selesnick discovered types of wavelet-like filters known as Slantlet filters or Slantlet transform (SLT) which can improve some of DWT properties, such as the time localization. The property of providing good time localization and better compression make Slantlet transform be better utilized for the different applications compared to DWT and DCT. The SLT structure is a bank of parallel filters, which are primarily an orthogonal DWT [6, 7, 8]. The parallel filters in this bank are denoted as; $h_i(n)$, $f_i(n)$, and $g_i(n)$, where (i) represents the SLT scale value. The filter length for scale (i) is (2^i), and this is almost true for filter-banks iterated. Whereas for Slantlet filter banks, this can be applied especially. The SLT have (2l) channels, where (l) is filter-banks scale. The $h_l(n)$ filter is called a lowpass filter and another filter which is adjacent to the lowpass is called $f_l(n)$ filter. Both filters, $h_l(n)$ and $f_l(n)$, are followed by down-sampling by (2l). The remaining branches (2l-2) which are$g_i(n)$ filter and its shifted time-reverse $g_i((2^{i+1}-1)-n)$, for i=1,. . .,l-1, are with down sampling is (2^{i+1}).

A three-scale iterated DWT filter-bank is considered in this paper. Such iterated DWT filter-bank and its equivalent structure are shown in Fig. 1. The SLT filter-bank structure is build based on the DWT equivalent structure, but the types of filters are occupied by different filters that aren't the products as shown in Fig. 2.

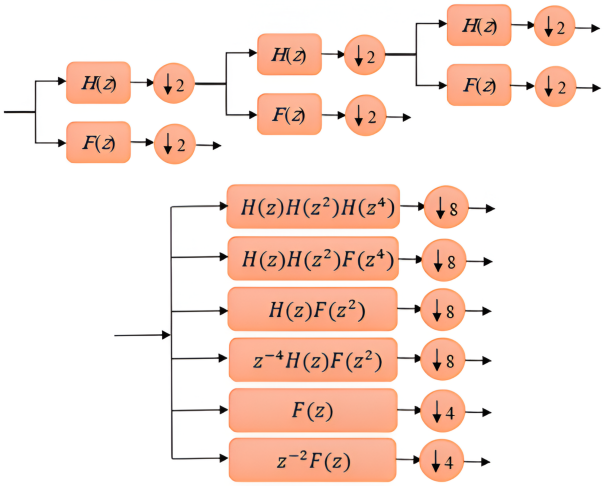


Fig. 1. The 3-scale DWT filter-banks with equivalent structure.

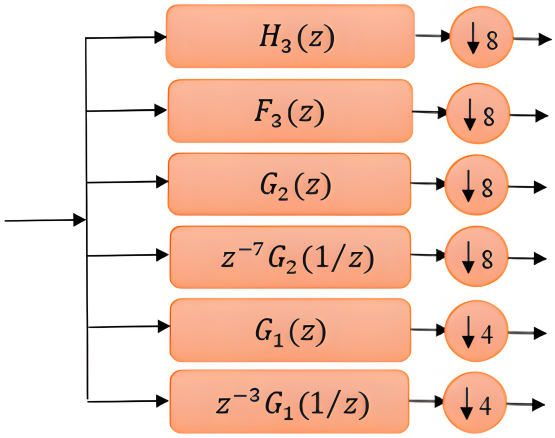


Fig. 2. The 3-scale SLT filter-banks structure.

With the additional degree of flexibility that's gotten by abandoning the product structure, filters of shorter length are designed to achieve both orthogonality properties and zero moment conditions. The 3-scale iterated Daubechies-2 (DB2) filter-banks (Fig.1) analyze the input signal at 3-scales with filters of length (4), (10), and (22), as illustrated on Fig. 3 (the left side). Whereas, the filters of SLT (which are G1, G2, H3, and F3, shown in Fig. 2) analyze the input signal at three scales with filters of length (4), (8), and (16) as illustrated on Fig. 3 (the right side). This reduction in length while

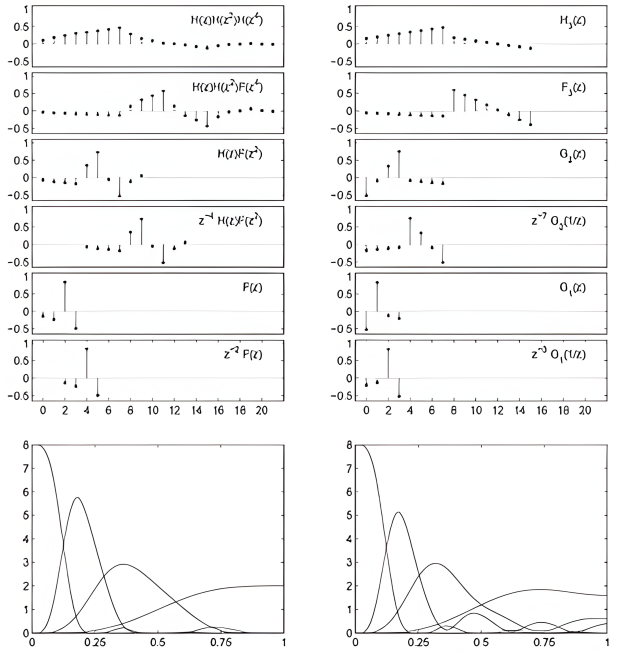


Fig. 3. Comparison of 3-scale iterated Daubechies-2 filter-banks (left-hand side) and 3-scale SLT filter-banks (right-hand side). Time responses (upper side) and frequency responses (lower).

maintaining moment property and desirable orthogonality, is possible because these filter-banks aren't constrained by the product structure that arises in the case of iterated filter-banks.

III. Less-complex realization of 3-scale SLT filters

A. Multiplierless filter representations

In this section, the number of coefficients of all SLT filters can be reduced and each coefficient of them is then represented based on the sum-of-power-of-two (SOPOT) method, leading to some reduction in the mathematical computations of SLT filters which may lead again to achieving a less complex realization. The SOPOT method is applied to represent the coefficients of the designed filters. Thus, in addition to the reduction in the multipliers block numbers, an easy overall implementation is accomplished by applying a restricted number of mathematical operations such as adders, subtracters and shifters blocks (without using multiplications).

On another side, in hardware, fewer mathematical blocks lead to lower power consumption and less-complex implementation significantly. So an efficient design of the system is confirmed, since the it can meet both reconfigurability and low complexity properties which are the main features of the practical applications that contribute in making the designed structure more efficient [9, 10]. The 3-scale of SLT have six filters; $H_3(z)$, $F_3(z)$, $G_2(z)$, $G_1(z)$, and two shifted time reverse ($z^{-7}G_2(1/z)$ and $z^{-3}G_1(1/z)$) as shown in Fig. 2.

The 3-scale of SLT filters have many coefficients which can be calculated by MATLAB program. A multiplier-less realization is adopted depended on shift right or shift left with adder or subtractor operations by apply SOPOT representation. This representation leads to producing less-complex hardware by reducing the number of required mathematical computations. In this paper, practically three highpass filters of the six SLT filters (F3, G2, and G1 filters) are only used to extract the features of the ECG signals. Due to their frequency response types. The other three filters will be cancelled because they can only produce small amounts of the ECG features which have no effect on the final diagnosis decision of the system designed. The following three tables: Table I, Table II, and Table III explain such multiplier-less realization for all coefficient's values of the 3-scale SLT selected filters.

To select a better wordlength, the error values in the SLT filters responses (magnitude and phase), which are built depending on both original and approximated coefficients values, are calculated as in Table IV, based on equations (9) and (10) of Ref. [11].

TABLE I.
$F_3(z)$ filter coefficients with its SOPOT representation.

Coefficients		5-bit Wordlength Representation of Coefficients	SOPOT Representation of Coefficients
h(0)	-0.0526	-0.0625	$-2^{\wedge}-4$
h(1)	-0.0665	-0.0625	$2^{\wedge}-4-2^{\wedge}-3$
h(2)	-0.0804	-0.0938	$2^{\wedge}-5-2^{\wedge}-3$
h(3)	-0.0943	-0.0938	$2^{\wedge}-5-2^{\wedge}-3$
h(4)	-0.1082	-0.1250	$-2^{\wedge}-3$
h(5)	-0.1221	-0.1250	$-2^{\wedge}-3$
h(6)	-0.1360	-0.1250	$2^{\wedge}-3-2^{\wedge}-2$
h(7)	-0.1500	-0.1563	$2^{\wedge}-3-2^{\wedge}-2-2^{\wedge}-5$
h(8)	0.5926	0.5938	$2^{\wedge}-4+2^{\wedge}-1+2^{\wedge}-5$
h(9)	0.4522	0.4375	$2^{\wedge}-1-2^{\wedge}-4$
h(10)	0.3118	0.3125	$2^{\wedge}-4+2^{\wedge}-2$
h(11)	0.1715	0.1563	$2^{\wedge}-5+2^{\wedge}-3$
h(12)	0.0311	0.0313	$2^{\wedge}-5$
h(13)	-0.1093	-0.1250	$-2^{\wedge}-3$
h(14)	-0.2497	-0.2500	$2^{\wedge}-2^{\wedge}-2^{\wedge}-1$
h(15)	-0.3901	-0.3750	$2^{\wedge}-3-2^{\wedge}-1$

TABLE II.
$G_2(z)$ filter coefficients with its SOPOT representation.

Coefficients		5-bit Wordlength Representation of Coefficients	SOPOT Representation of Coefficients
h(0)	-0.5062	-0.5000	$-2^{\wedge}-1$
h(1)	-0.0874	-0.0938	$2^{\wedge}-5-2^{\wedge}-3$
h(2)	0.3314	0.3125	$2^{\wedge}-4+2^{\wedge}-2$
h(3)	0.7502	0.7500	$2^{\wedge}-2+2^{\wedge}-1$
h(4)	-0.0793	-0.0938	$2^{\wedge}-5-2^{\wedge}-3$
h(5)	-0.1078	-0.1250	$-2^{\wedge}-3$
h(6)	-0.1362	-0.1250	$2^{\wedge}-3-2^{\wedge}-2$
h(7)	-0.1646	-0.1563	$2^{\wedge}-4-2^{\wedge}-2+2^{\wedge}-5$

TABLE III.
$G_1(z)$ filter coefficients with its SOPOT representation.

Coefficients		5-bit Wordlength Representation of Coefficients	SOPOT Representation of Coefficients
h(0)	-0.5117	-0.5000	$-2^{\wedge}-1$
h(1)	-0.8279	0.8125	$1-2^{\wedge}-3-2^{\wedge}-4$
h(2)	-0.1208	-0.1250	$-2^{\wedge}-3$
h(3)	-0.1954	-0.1875	$2^{\wedge}-4-2^{\wedge}-2$

TABLE IV.
Maximum and average deviation values of the magnitude and phase responses based on number of bits representation.

No. of Bits (Wordlength)			SLT filters		
			$F_3(z)$	$G_2(z)$	$G_1(z)$
3	Magnitude Response Error	ΔAva	0.0892	0.0888	0.0483
		Max (Mag_{error})	0.2582	0.1885	0.0150
	Phase Response Error	ΔAva	0.3363	0.1467	0.2191
		Max ($Phase_{error}$)	3.0467	3.1051	3.0681
5	Magnitude Response Error	ΔAva	0.0245	0.0203	0.0180
		Max (Mag_{error})	0.0572	0.0467	0.0298
	Phase Response Error	ΔAva	0.0459	0.0664	0.0050
		Max ($Phase_{error}$)	0.9016	3.1321	0.0116
7	Magnitude Response Error	ΔAva	0.0053	0.0048	0.0049
		Max (Mag_{error})	0.0078	0.0091	0.0077
	Phase Response Error	ΔAva	0.0085	0.0237	0.0060
		Max ($Phase_{error}$)	0.3534	3.1335	0.2958

It is Known that to implement the digital filters in a programmable logic device like FPGA, there are some parameters which are dependent on wordlength of the filter coefficient, such as the area, consumption power, and mathematical operations. Due to that, the coefficient wordlength should be as short as possible but still enough to achieve the given filter specifications.

The best-selected implementation of the SLT filters on FPGA is achieved by a proper choice of wordlength required to represent the filter coefficients. The filters are rebuilt using coefficients with different wordlengths. The maximum and average error values of the modified and original magnitudes and phase responses of each SLT filter coefficients are then calculated and compared using 3, 5, and 7-bits wordlength cases as shown in Table IV. Among different error values in Table IV, it is clear that the most acceptable error values of the responses are the values at wordlength of 5-bits representation, where the maximum error value in magnitude response of the filters, have not exceeded 5.72% replacing error value around 25.8% for 3-bits representation which mean that the response is improved by more than 20%. Also, with regard to the average error, it is noticed that using 5-bits to represent the coefficients can reduce the error by about 27% compared with that of using 3-bits. Accordingly, the accepted error values in Table IV motivate us to choose 5-bit wordlength representation of coefficients.

B. Multiplierless filter reductions

In this paper, as it is illustrated in Table I, Table II and Table III, the SLT filters are designed using a method which makes the consuming power of the designed system as low as possible. This may be achieved by reducing the mathematical operations, or in other words, modifying the filter's coefficient values to the nearest possible numbers where all SLT coefficients can be represented based on SOPOT method. Also, choosing the 5 bits to represent the coefficients with acceptable error values can lead to some reduction in the total number of the coefficients to be designed with, reflecting lower complexity and more efficient system. In Table I, the F3 filter has 16 coefficients that are then reduced to be only 10 coefficients which can be represented in multiplier-less manners. While the G2 filter has 8 coefficients which are reduced to be only 6 coefficients as represented in multiplier-less manners as illustrated in Table II. In Table III, the G1 filter has 4 coefficients which is also possible to be represented based on a multiplier-less manner.

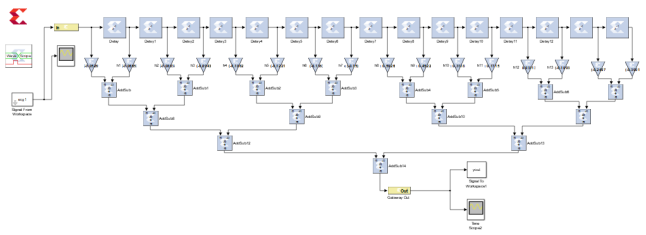
IV. FPGA IMPLEMENTATION RESULTS

The proposed designed structure provides an efficient hardware architecture for arrhythmia electrocardiogram (ECG) classification system by the artificial neural network (ANN). The best choice for implementing the proposed classification system is the FPGA devices, which combine the high performance of ASICs and the flexibility of DSPs. The Xilinx system generator is a high-level tool that allows the use of MATLAB/Simulink environment to create and verify FPGA designs in a quick and easy way [12, 13]. In this section, simulation results of 3-scale SLT filters are presented. The

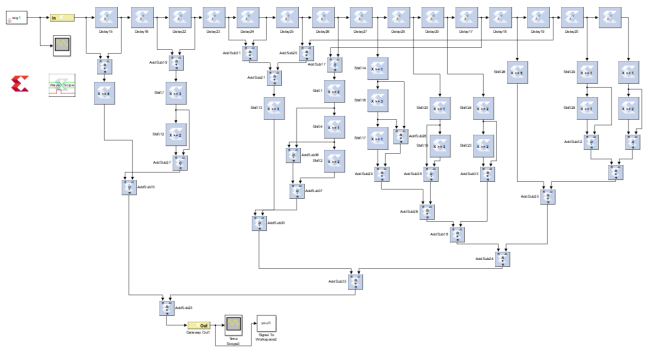
filter-banks are implemented based on Xilinx System Generator. The FPGA implementations are accomplished on Xilinx SPARTAN-6 XC6SLX16TM.

A. FPGA implementation results of F3 filter

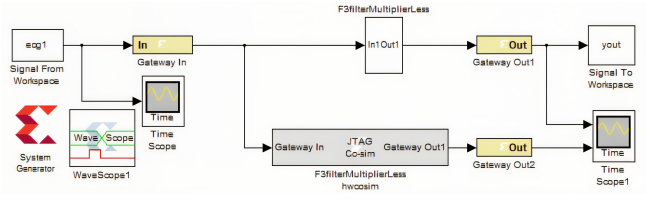
3-scale SLT filters can be used to get the significant features of the ECG signals. One of the important SLT filters is the F3 filter, which contains the highest information of ECG signals. The filter implemented based on the original multipliers and also based on SOPOT method for proving an efficient performance of the system designed with less-complexity. The obtained features of the two implemented structures in Fig. 4, can be compared throughout measuring the performance of the designed system by calculating the maximum and average errors. The recorded error values of the F3 filter are as follows: the maximum error value reaches 5.49% whereas the averaging error value is 1.15 %.



(a) F3 filter structure built based on original coefficients.



(b) F3 filter structure built based on SOPOT representation.



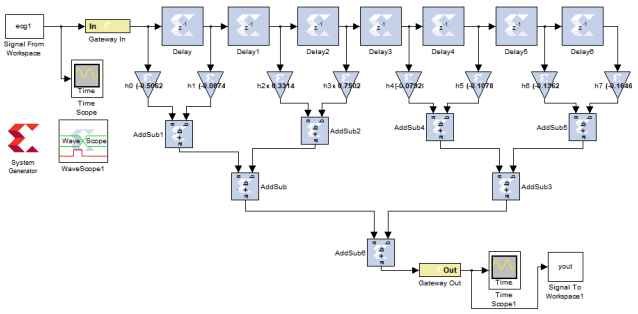
(c) Hardware Xilinx system generation of F3 filter..

Fig. 4. The F3 filter implementation based on SOPOT.

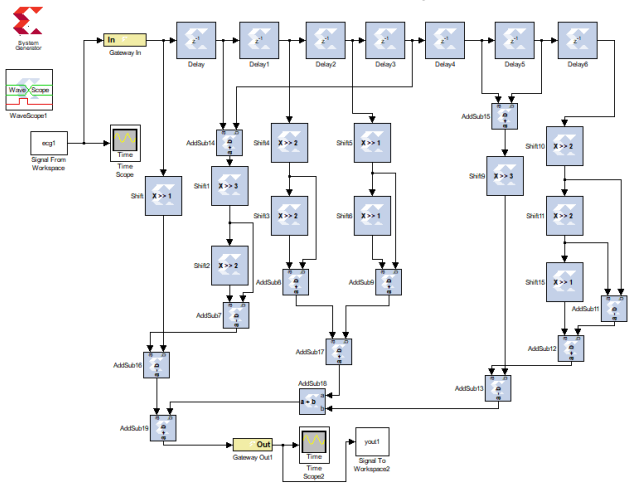
The results of F3 filter pipeline implementations on spartan-6 FPGA are summarized below as in Table V, for two cases; with original multipliers and multiplierless representation.

TABLE V.
Device utilization comparison summary of F3 filter when the filter is represented based on original multipliers and multiplierless representation.

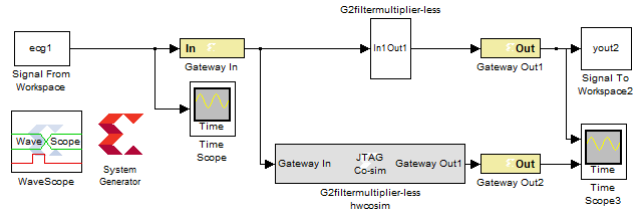
Device Utilization Summary	Original Multipliers (F3 filter)			Multiplierless (F3 filter)		
Slice Logic Utilization	Used	Available	Utilization	Used	Available	Utilization
Slice Registers Number	252	18,224	1%	238	18,224	1%
Slice LUTs Number	1,496	9,112	16%	528	9,112	5%
Occupied Slices Number	468	2,278	20%	152	2,278	6%
Number of MUXCYs used	1,128	4,556	24%	476	4,556	10%
LUT Flip Flop pairs used Number	1,511			565		
bonded IOBs Number	53	232	22%	40	232	17%
Average - Fanout of Non-Clock Nets	3.25			2.04		
Maximum Frequency	375.094MHz			375.094MHz		



(a) G2 filter structure built based on original coefficients.



(b) G2 filter structure built based on SOPOT representation.



(c) Hardware Xilinx system generation of G2 filter.

Fig. 5. The G2 filter implementation based on SOPOT.

TABLE VI.
Device utilization comparison summary of G2 filter when the filter is represented based on original multipliers and multiplierless representation.

Device Utilization Summary	Original Multipliers (G2 filter)			Multiplierless (G2 filter)		
Slice Logic Utilization	Used	Available	Utilization	Used	Available	Utilization
Slice Registers Number	119	18,224	1%	110	18,224	1%
Slice LUTs Number	734	9,112	8%	264	9,112	2%
Occupied Slices Number	246	2,278	10%	74	2,278	3%
Number of MUXCYs used	540	4,556	11%	244	4,556	5%
LUT Flip Flop pairs used Number	741			266		
bonded IOBs Number	52	232	22%	38	232	16%
Average - Fanout of Non-Clock Nets	3.26			2.02		
Maximum Frequency	306.748MHz			375.094MHz		

It's clear that the proposed design led to reducing the used slice numbers where the number of occupied slices decreased about 30% in the case of the multiplierless implementation. Therefore, the F3 filter with multiplierless representation consumes fewer resources and consequently less-power.

B. FPGA implementation results of G2 filter

Same procedure of section IV.A, can be followed for the second SLT filter which is the G2 filter.Figure 5 illustrates all the co-simulation and implementation results of G2 filter. The deviation and maximum error values calculated to be 0.6% as an averaging error value and 0.1% as a maximum error value.

Same as in the procedure of F3 filter, the implementation results of G2 filter are summarized in Table VI. The efficient proposed design led to reducing the used slices on FPGA, where the number of occupied slices for G2 filter in case of multiplierless implementation is decreased a round 30% compared with the multiplier implementation.

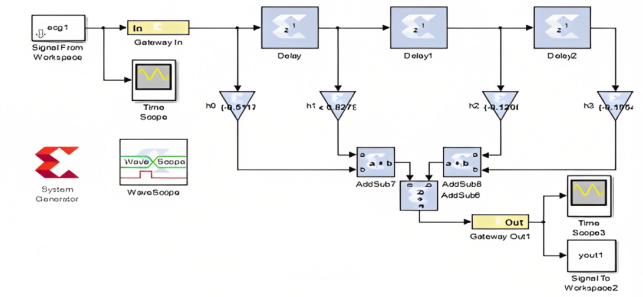
C. FPGA implementation results of G1 filter

Again the same procedures of the previous sections can be followed for the third SLT filter which is the G1 filter. Figure 6 illustrates all the results of the G1 filter. The maximum and deviation error values are calculated to be 0.01% as an averaging error value and 0.14% as a maximum error value.

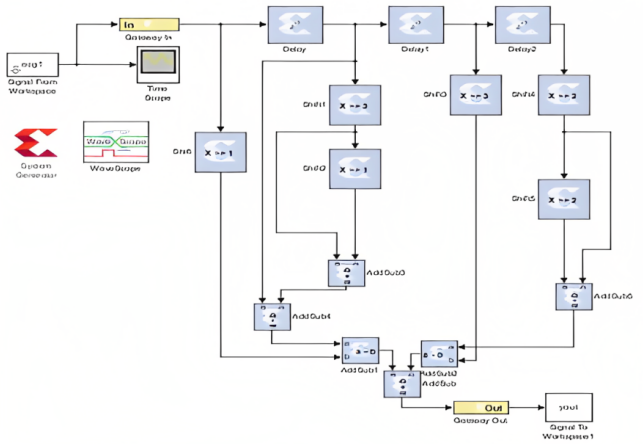
Here also the FPGA implementation results of G1 filter for the two cases (with original multipliers and multiplierless) are summarized in Table VII. The percentage of improvement (occupied slices) is 20% in case of building the G1 filter based on multiplierlss representation compared with multiplier representation.

TABLE VII.
Device utilization comparison summary of G1 filter when the filter is represented based on original multipliers and multiplierless representation.

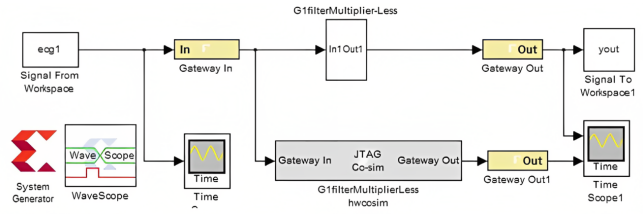
Device Utilization Summary	Original Multipliers (G1 filter)			Multiplierless (G1 filter)		
Slice Logic Utilization	Used	Available	Utilization	Used	Available	Utilization
Slice Registers Number	51	18,224	1%	44	18,224	1%
Slice LUTs Number	345	9,112	3%	120	9,112	1%
Occupied Slices Number	118	2,278	5%	34	2,278	1%
Number of MUXCYs used	244	4,556	5%	112	4,556	2%
LUT Flip Flop pairs used Number	352			128		
bonded IOBs Number	51	232	21%	36	232	15%
Average - Fanout of Non-Clock Nets	3.45			1.98		
Maximum Frequency	375.094MHz			375.094MHz		



(a) G1 filter structure built based on original coefficients.



(b) G1 filter structure built based on SOPOT representation.



(c) Hardware Xilinx system generation of G1 filter.

Fig. 6. The G1 filter implementation results based on SOPOT.

V. ECG CLASSIFICATION; ALGORITHM AND RESULTS

ECG signals classification plays a significant role in the diagnoses of heart diseases which faces a strong challenging problems due to its importance. Different methods for ECG classification are available, but among all the classifiers, the artificial neural networks become the most common used one for ECG classification [14, 15]. The physionet data-base of biomedical signals is used as the source of ECG signals, namely the MIT-BIH ECG data-base [16]. Features extraction of ECG signals are the key for classification. Fig.7 illustrates the proposed ECG classification system where the outputs of SLT filters (F3, G2, and G1) represent the most important features of an ECG signals, containing the sudden changes of the signal which are classified after that based on a neural network system. An easy way to design the ANN algorithm is to use the pattern recognition tool, which is a toolbox available in the MATLAB command window. The process of training is achieved with two layers, one hidden with four neurons and another output layer with five neurons. The activation function of hidden layer is a tan-sigmoid whereas the output layer is softmax. The classifier of Fig. 7 is designed

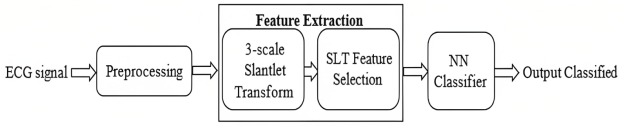


Fig. 7. The ECG classification proposed system.

and trained to accept five cases of ECG diseases (Normal, Right Bundle Branch Block (RBBB), Left Bundle Branch Block (LBBB), Tachycardia, and Myocardial Infarction). The MATLAB/Simulink results of the designed ANN classifier are shown in Table VIII, where the total accuracy of the training and validation procedure using five ECG signals is 100% while the testing accuracy is 90% and the overall accuracy is 98.5%.

TABLE VIII.
Classifier accuracy values of output classes.

Process	ANN Accuracy of Output Cases					Total Percentages
	Normal	RBBB	LBBB	Tachycardia	Myocardial Infarction	
Training	100	100	100	100	100	100%
Validation	100	100	100	100	100	100%
Testing	100	100	100	50	100	90%
Average	100	100	100	92.3	100	98.5%

From the classification results shown in Table VIII, it's clear that the robustness of SLT for features extraction of ECG signals give some impressive results compared with the classification results of some other recent works in this field. The classification performance of the proposed method is compared with other works. This comparison is illustrated in the Table IX.

TABLE IX.
Comparison between the proposed ECG classification and other classifications

Literature works	Features extraction methods	Classifier	Accuracy Percentages (%)
Ref. [17]	Cumulant + PCA	ANN	94.52%
Ref. [18]	DWT+PCA	SVM-RBF	96.92%
Ref. [19]	DWT	ANN	96.67%
Ref. [20]	BLWDF	ANN	96.30%
Ref. [21]	3-scale SLT based on Original Multipliers representation	ANN	98.40 %
Proposed	3-scale SLT based on SOPOT representation	ANN	98.50%

From Table IX, it's clear that the features extraction of ECG signals based on 3-scale SLT filters with SOPOT representation led us to a less-complex classifier system. In addition, it's an exploit of the most of ECG features which made the classification process be easy and accurate.

VI. CONCLUSION

In this paper, an efficient ECG classification system has been introduced. The feature extraction of ECG signals has been made depended on 3-scale SLT filters with SOPOT representation, leading to less complexity in realization and implementation. The global maximum deviation in the magnitude response has appeared not being exceeding 2.45 %, while it has reach 4.59 % in the phase response. FPGA results have proved that the designed system which is realized based on SOPOT representation are more efficient with less-complex implementation cost compared with those realized with original multipliers representation (maximum error has reach 5.49 % and deviation error has record 1.15 %).

The proposed classifier system is capable of distinguishing the normal ECG case and other four different diseases with an overall accuracy of classification reach to 98.50 %. Such results have made this system overcome other recent works. It should be noted that the performance of the proposed system can be enhanced using better features and also more diverse electrocardiogram beats for training and testing.

CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

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