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Design and Simulation of Reduced Switch 31-Level Multilevel Inverter Topology for PV Application

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Abstract
This paper presents a design of a low cost, low loss 31-level multilevel inverter (MLI) topology with a reduce the number of switches and power electronic devices. The increase in the levels of MLI leads to limiting the THD to the desired value. The 31-level output voltage is created using four PV sources with a specific ratio. The SPWM is used to control the gating signals for the switches of MLI. The PV system is integrated into the MLI using a boost converter to maximize the power capacity of the solar cells and the Incremental Conductance (IC) algorithm is employed for maximum power point tracking (MPPT) of the PV system. Simulation results of 31-level MLI indicate the THD of voltage and current waveforms are 3.73% within an acceptable range of IEEE standards.

Keywords
Incremental Conductance (IC) Algorithm, Multilevel Inverter (MLI), Photovoltaic (PV), Total Harmonic Distortion (THD).

I. Introduction

Multi-level inverters (MLIs) are commonly used in various electrical engineering applications such as solar energy systems and variable speed drives. MLIs provide high power operation capability and many benefits, including reduced harmonics, improved power quality, reduced electromagnetic interference, and lower switching losses. The increased demand for higher-power appliances has led to MLIs being widely used in many industrial applications and have vast potential for research and development [1] and [2]. MLIs offer numerous advantages over 2-level inverters, generating a superior sinusoidal output, resulting in a significant reduction in THD. As a result, MLIs minimize the need for extensive filtering, while simultaneously exhibiting higher efficiency, and compact stress on switches [3]. The modular topology of cascaded H-bridge (CHB) MLIs enables them to handle high voltage and power levels effectively. However, this advantage comes with the drawback of requiring a larger number of power semiconductor switches [4]. As a result, switching losses are increased, leading to larger circuit sizes and higher costs. To address these issues, alternative MLIs have been developed with the specific goal of reducing the number of devices. These alternative topologies are known as MLIs with reduced devices [5]. The reduction in the number of switches in a circuit leads to decreased switching losses and lower requirements for driver and snubber circuits [6].

Similar topologies have been proposed in related domains as well there has been a proliferation of proposed topologies for cascaded multilevel inverters, utilizing diverse control techniques [7, 8]. Additionally, several symmetric cascaded multilevel inverter configurations have been introduced and documented in [9-11]. These topologies offer significant advantages, notably the utilization of low DC voltage sources, which have a substantial impact on the cost-effectiveness of inverters. Conversely, certain topologies rely on a larger number of bidirectional switches, leading to the drawback of requiring

a greater quantity of IGBTs.

The topology presented in [9] introduced a fundamental structure comprising nine switches, resulting in 15-levels. Conversely, [10] presented a symmetric arrangement to achieve even higher levels, but this approach necessitates additional capacitors and the voltages across the devices are higher in the design. In [11], a topology with a high level per component ratio was proposed, which has been tested for design and performance parameters using several sources. This particular topology is suited for PV (photovoltaic) systems. In [12], a higher MLI that is appropriate for high and low switching frequencies was introduced. In [13], the author has presented reduced cascaded multilevel inverter (MLI) topologies aimed to minimize the number of devices and the stress voltage on the power switches. However, the aforementioned works did not include the photovoltaic system within the MLI configuration. In addition, the minimization of components was not considered to realize the acceptable range of THD.

This work is organized as follows. Section 2 presents the structure and principal works of the proposed reduced switch 31-level MLI topology. Section 3 describes the MPPT of PV based on the IC algorithm. Section 4 presents the results and discussions. Section 5 summarizes the results of 31-level MLI with PV integration.

II. The Proposed Reduced Switch 31-Level MLI Topology

A. *The structure of 31-level MLI*

The proposed structure of 31-level MLI that is shown in Fig. 1 consists of eight switches (S1 to S8), four diodes (D1 to D4), and four modules of the photovoltaic system denoted as PV1, PV2, PV3, and PV4. The desired 31-level output voltage is achieved by utilizing a configuration of four PV sources in a ratio of 1 : 2 : 3 : 4. The magnitudes of the four modules PV system are PV1, PV2 = 2PV1, PV3 =4PV1, and PV4 = 8PV1, respectively.

The principal operation of the 31-level MLI can be analyzed by the pulses of switches during the operation of each one. Fig. 2 shows the schematically predictable output voltage waveform of the 31-level MLI for resistive load with the required pulsing signal for switches (S1 to S8) that will applied using the SPWM technique. Table I illustrates the state operations of switches to produce the 31-level MLI during one period where switch state '1' indicates a closed switch and '0' indicates an open switch. Fig. 3 shows the modes (M1-M16) operation of the proposed 31-level MLI for a positive cycle. The modes of operation of the negative cycle of MLI are the same positive cycle except (S5=S8=0 and S6=S7=1).

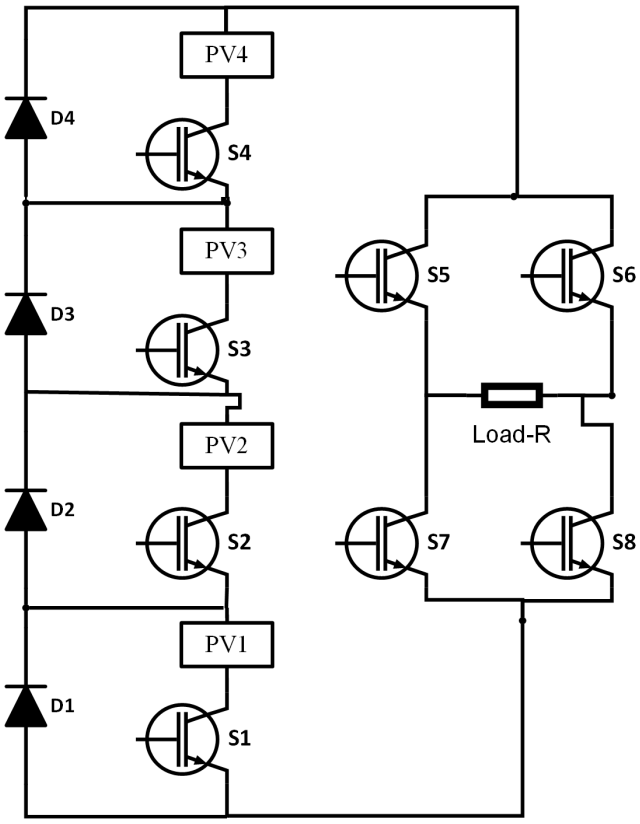

Fig. 1. Schematic structure of proposed 31-level MLI with reduced switches for resistive load.

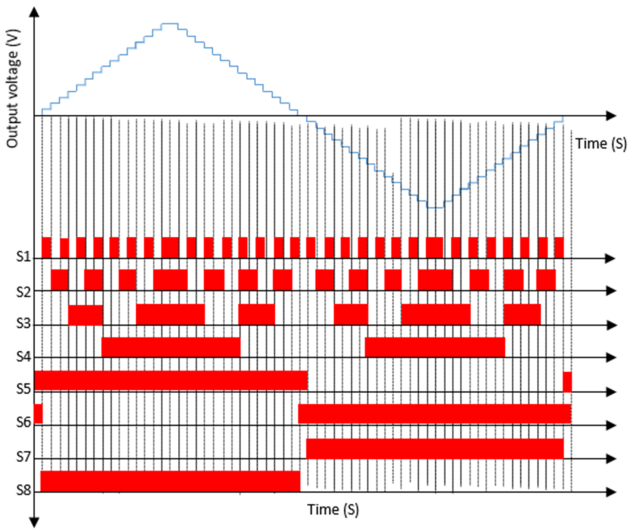

Fig. 2. Schematic expected 31-level output voltage waveform with gate signals for switches (S1 to S8) for resistive load.

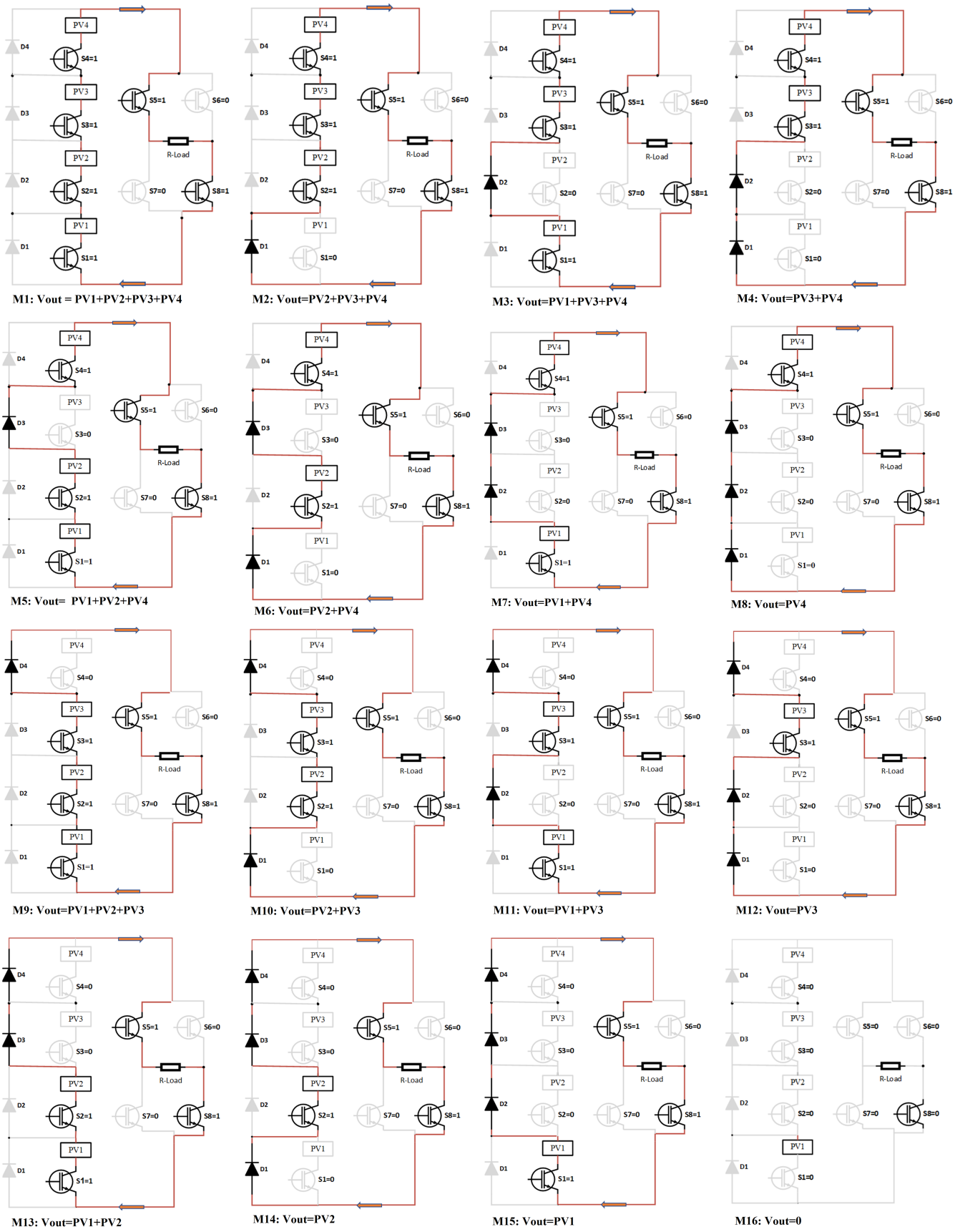

Fig. 3. The modes (M1-M16) operation of proposed 31-level MLI for a positive cycle.

TABLE I.
THE SWITCHES (S1 TO S8) STATE OF THE 31-LEVEL MLI

Switches state								Output voltage
S1	S2	S3	S4	S5	S6	S7	S8	Activate PV sources
1	1	1	1	1	0	0	1	PV4+PV3+PV2+PV1
0	1	1	1	1	0	0	1	PV4+ PV3+PV2
1	0	1	1	1	0	0	1	PV4+ PV3+PV1
0	0	1	1	1	0	0	1	PV4+PV3
1	1	0	1	1	0	0	1	PV4+PV2+PV1
0	1	0	1	1	0	0	1	PV4+PV2
1	0	0	1	1	0	0	1	PV4+PV1
0	0	0	1	1	0	0	1	PV4
1	1	1	0	1	0	0	1	PV3+PV2+PV1
0	1	1	0	1	0	0	1	PV3+PV2
1	0	1	0	1	0	0	1	PV3+PV1
0	0	1	0	1	0	0	1	PV3
1	1	0	0	1	0	0	1	PV2+PV1
0	1	0	0	1	0	0	1	PV2
1	0	0	0	1	0	0	1	PV1
0	0	0	0	0	0	0	0	——-
1	1	1	1	0	1	1	0	-PV4-PV3-PV2-V1
0	1	1	1	0	1	1	0	-PV4- PV3-PV2
1	0	1	1	0	1	1	0	-PV4-PV3-PV1
0	0	1	1	0	1	1	0	-PV4-PV3
1	1	0	1	0	1	1	0	-PV4-PV2-PV1
0	1	0	1	0	1	1	0	-PV4-PV2
1	0	0	1	0	1	1	0	-PV4-PV1
0	0	0	1	0	1	1	0	-PV4
1	1	1	0	0	1	1	0	-PV3-PV2-PV1
0	1	1	0	0	1	1	0	-PV3-PV2
1	0	1	0	0	1	1	0	-PV3-PV1
0	0	1	0	0	1	1	0	-PV3
1	1	0	0	0	1	1	0	-PV2-PV1
0	1	0	0	0	1	1	0	-PV2
1	0	0	0	0	1	1	0	-PV1

B. The power losses of 31-level MLI

The total power losses that occur in switches of MLI are divided into two types switching and conduction losses. The conduction losses (P_{cond}) of switches (IGPT) occur around 2Π period and it can be estimated as follows [14]:

$$P_{\text{cond}} = \sum_{K=1}^{Nsw} \frac{1}{2\pi} \int_0^{2\pi} \left(i(t) Vsw + i^{\beta}(t) Rs \right) dt \tag{1}$$

Where V_{sw} is the voltage drop across the switches when being on state, Rs is the switch resistance in on state, N_{sw} is the number of switches in MLI, $i(t)$ is the output current, and β is constant value estimate from the switch datasheet.

The switching losses (P_s) occur during the on and off state of working of switches and they can be determined as follows:

$$P_{\text{s, }ON} = \frac{1}{T} \int_0^{t_{\text{ON}}} i(t) Vswdt = \frac{1}{6T} \left[It_{\text{ON}} Vsw \right] \tag{2}$$

$$P_{\text{s, OFF}} = \frac{1}{T} \int_0^{t_{\text{OFF}}} i(t) Vswdt = \frac{1}{6T} \left[It_{\text{OFF}} Vsw \right] \tag{3}$$

Where T is the total period time, $P_{s,ON}$ is the switching losses in ON-state, $P_{s,OFF}$ is the switching losses in OFF-state, and t_{OFF}, t_{ON} are the OFF and ON states period of switch respectively. Therefore, the total switching losses can be found as follows:

$$P_s = P_{\text{s, ON}} + P_{\text{s, OFF}} \tag{4}$$

Hence, the total power loss (P_{loss}) is the sum of switching losses and conduction losses.

$$P_{\text{loss}} = P_s + P_{\text{cond}} \tag{5}$$

Furthermore, the efficiency (η) of the proposed 31-level MLI can be calculated as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{loss}} P_{\text{out}}} \tag{6}$$

and the output power can be found as:

$$P_{\text{out}} = V_{\text{rms}} * I_{\text{rms}} \tag{7}$$

C. The SPWM of 31-level MLI

The gating signal for switches (S1 to S8) of the 31-level MLI is created by utilizing the SPWM technique. To achieve a 31-level output waveform, the modulation technique being proposed involves the utilization of fifteen triangle carrier signals along with one reference signal (sine wave) modulating signal [15]. The proposed SPWM for 31-MLI is constructed in the MATLAB program as shown in Fig. 4.

In this work, the MATLAB program is used to implement the Simulink model of 31-level MLI with SPWM and PV system as shown in Fig. 5. The PV1 module in Fig. 5 is illustrated in Fig. 6. As shown in this figure, the PV panel is supplied to converter to extract the maximum power possible from the PV system. The PV2, PV3, and PV4 are all designed in the same way with different magnitudes of out voltage which equals: PV2=2PV1, PV3=4PV1, and PV4=8PV1.

To maximize the power capacity of the PV, the output of the PV is connected to a boost converter (mentioned in Fig. 6), which supplies the power to the inverter (see Fig. 5). The duty cycle of the converter is used to regulate the power that supplied to 31-level MLI. In this particular study, the duty cycle was controlled using the IC algorithm to extract the desired power of the PV panel that is supplied to the inverter.

III. MPPT OF PV BASED ON IC ALGORITHM

The goal of the IC algorithm is to identify the peak of the power curve to detect the MPPT. At the point of maximum power, the curve slope of the PV is zero, represented by $(dP/dV) = 0$ as shown in Fig. 7, where P represents power

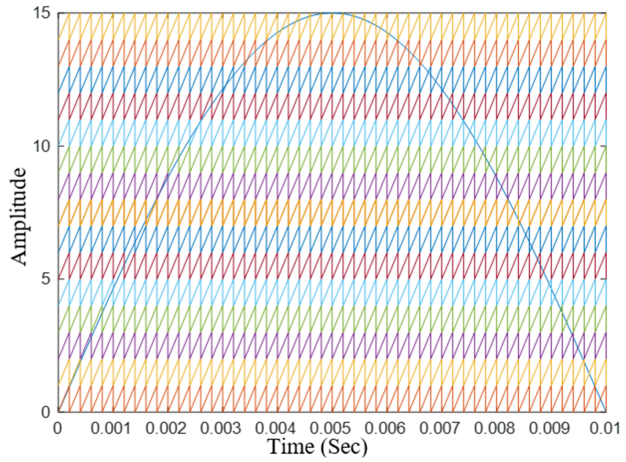

Fig. 4. The triangle carrier signals with a reference signal (sine wave) for switches (S1 to S8) for 31-level MLI.

and V represents voltage. The IC method utilizes the instantaneous conductance (I/V) and the incremental conductance (dI/dV). By analyzing the relationship between these values, the operating point of the P-V curve can be determined [16]. Equations (8) through (12) show the principle work of the IC algorithm which depends on the changing ratio of power to

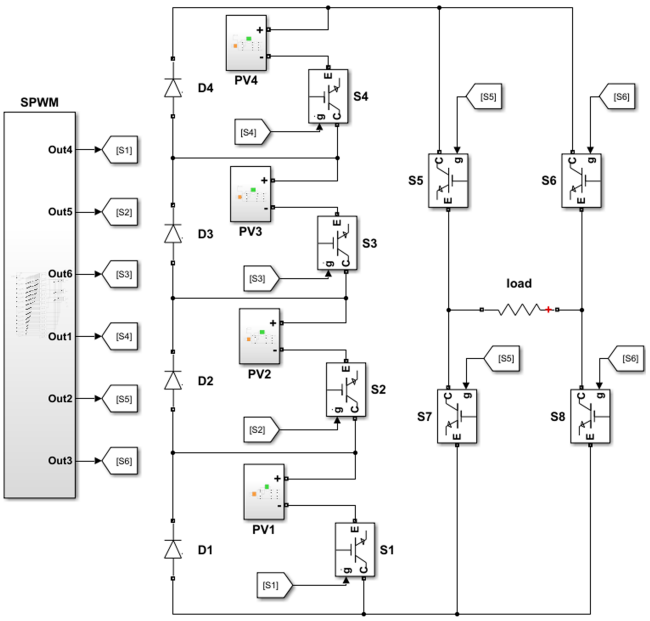

Fig. 5. MATLAB Simulink model of 31-level MLI topology for resistive load with signal gate pulsing (SPWM) for switches.

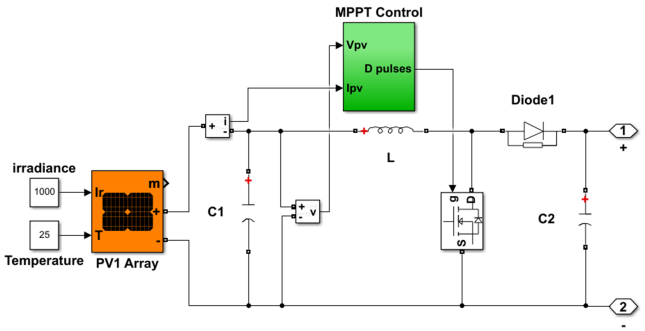

Fig. 6. The PV1supplied to boost converter with MPPT control (IC algorithm) of subsystem Fig. 5.

voltage to tune the duty cycle of the converter.

$$\frac{dP}{dV} = \frac{d(VI)}{dV} = I + V\left(\frac{dI}{dV}\right) = 0 \text{ at the MPPT} \tag{8}$$

When $\frac{dP}{dV} = 0$ the MPPT is reached and yield

$$\frac{dI}{dV} = -\frac{I}{V} \tag{9}$$

$$\frac{dp}{dV} > 0 \text{ then } V_{\text{mpp}} > V_P \tag{10}$$

$$\frac{dp}{dV} = 0 \text{ then } V_{\text{mpp}} = V_P \tag{11}$$

$$\frac{dp}{dV} < 0 \text{ then } V_{\text{mpp}} < V_P \tag{12}$$

where V_{mpp} and V_P are the voltages at maximum power point and photovoltaic voltage respectively.
The operating IC algorithm can be simplified in the flowchart that is shown in Fig. 8, while Fig. 9 depicts the corresponding Simulink model of the IC algorithm. This method adjusts the reference voltage by increasing or decreasing the duty cycle until the condition defined by (11) is satisfied.

IV. Results and Discussions

The simulation of the reduced switch 31-level MLI with PV system was implemented using MATLAB-Simulink program (see Figs. 5 and 6) and the IC algorithm was utilized to control the duty cycle in the simulation. A 31-level output voltage and current waveform were generated in this simulation and the signal gating of switches was accomplished using SPWM. In the simulation, the pulse signals were implemented with a

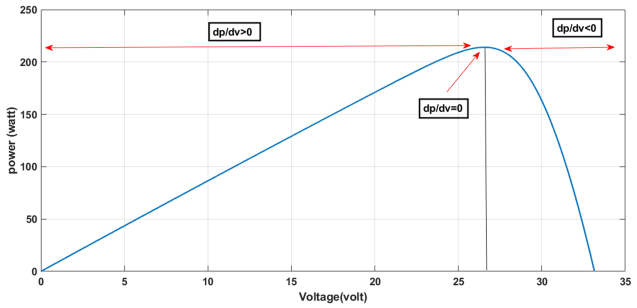

Fig. 7. The P-V curve for the IC algorithm.

carrier frequency of 5 kHz and the reference signal is 50 Hz (see Fig. 4), the design 31-level MLI was tested with a 100Ω resistive load. The parameters of the one module of the PV system (The Kyocera solar KD215GX-LPU) are mentioned in Table II. Fig. 10 illustrates the output voltage of the Photovoltaic (PV1) system with a boost converter and IC algorithm, which was generated at $1000\,W/m^2$. This output voltage was then supplied to a multilevel Inverter. Fig. 11 shows the output and input power of the boost converter at $1000\,W/m^2$ with the IC algorithm and the efficiency of this converter is 97.8%. The MLI produced a 31-level output voltage, reaching a peak magnitude of $1500V$, and each voltage step is $100\,V$, as shown in Figs. 12a and 12b. The voltage across switches (S1 to S4) of MLI is shown in Fig. 13.

To evaluate the performance of the MLI, the load current

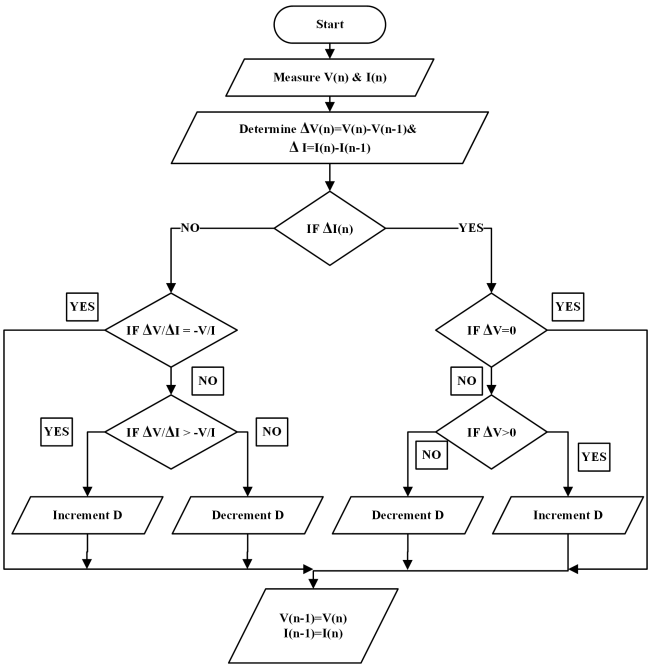

Fig. 8. Schematic flow chart operation of the IC algorithm.

TABLE II.
THE KYOCERA SOLAR KD215GX-LPU ELECTRICAL SPECIFICATION

Quantity	Value	Units
V_{mpp}	26.6 V	V
I_{mpp}	8.09A	A
P_{mpp}	215.194W	W
$V_{(o.c)}$	33.2V	V
I_{sc}	8.78A	A
K_i	(0.02±0.015) $mA/^\circ C$	$mA/^\circ C$
K_v	-(93±10) $mV/^\circ C$	$mV/^\circ C$
N_S	54	—-

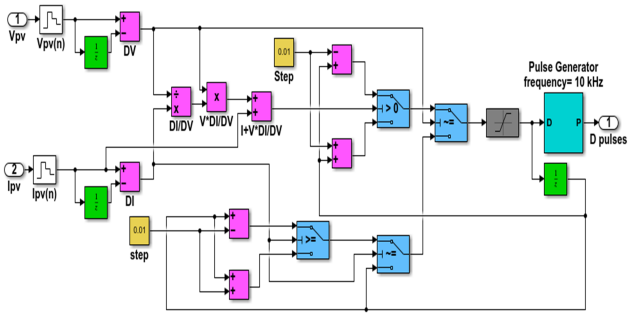

Fig. 9. MATLAB simulink model of the IC algorithm for tuning the duty cycle (D pulse).

waveform was simulated under a load of 100 ohms as shown in Fig. 14 and the efficiency obtained from the proposed inverter is 98.6%. Moreover, to show the quality of the output voltage and current waveforms, the harmonic spectrum of the voltage was obtained as shown in Fig. 15. This spectrum offers insights into the presence of harmonic components in the simulated output voltage waveform. The ratio of the THD that obtained from the voltage and current waveforms mentioned in Fig. 15 is 3.73%, which shows the efficiency of the MLI that is used with the PV system.

To prove the validation of the proposed MLI, the simulation was replicated under different conditions (irradiance $200\,W/m^2$ and temperature $25^\circ C$)as is shown in Figs. 16 through 19. These figures show the effectiveness of the proposed 31-level MLI to produce output voltage and current waveforms with the acceptable range of THD at different irradiance. The effect of variation irradiance from $1000\,W/m^2$ to $200\,W/m^2$ will reduce the power that supplies to inverter. To show the effectiveness of the proposed 31-level MLI is tested under changing temperature ($40^\circ C$) on PV system and the type of load ($50\,\Omega + 100\,mH$). The effect of increase of the temperature on PV system will decrease the voltage that is supplied to MLI as shown in Fig. 20. Fig. 21 shows the

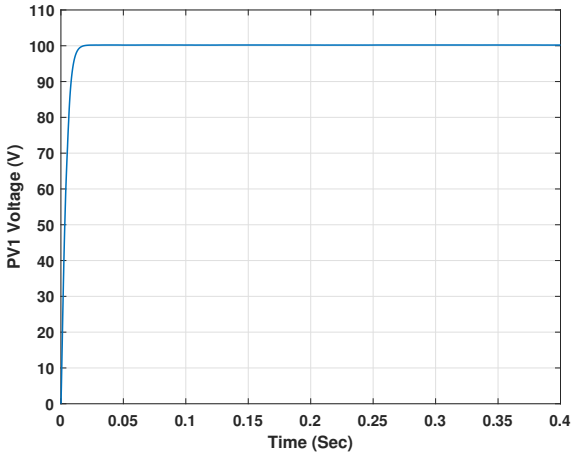

Fig. 10. Output voltage waveform of PV1 at $1000\,W/m^2$ and $25°C$ with a boost converter and IC algorithm.

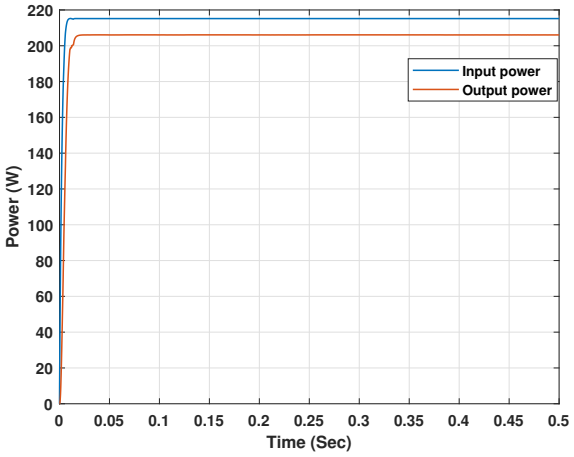

Fig. 11. The output and input power of the boost converter at $1000\,W/m^2$ and $25°C$ with the IC algorithm.

TABLE III.
COMPARISON OF REDUCED SWITCH 31-LEVEL MLI TOPOLOGY WITH RECENT TOPOLOGIES

Topologies	2025	NL	NS	ND	NDR	NC	NSO
[17]	2019	31	16	2	16	4	2
[18]	2019	31	10	-	10	-	4
[19]	2020	13	12	-	11	2	1
[20]	2020	31	18	-	18	4	2
[21]	2020	31	12	-	10	4	3
[22]	2021	13	14	1	14	3	1
[23]	2023	15	7	3	5	-	3
Proposed	-	31	8	4	6	-	4

current waveform at RL load and conditions $1000\,W/m^2$ and $40°C$. A detailed comparison is conducted on various performance parameters for 31-level multilevel inverters (MLI) in comparison to other recent topologies. The parameters considered in this analysis include the number of switch count (N_S), number of capacitors (N_C), number of diode (N_D), number of driver circuits (N_{DR}), and number of Voltage Sources (N_{SO}). The comparison results are illustrated in Table III.

V. CONCLUSION

This work introduced a multilevel inverter (MLI) with a simplified component topology, resulting in 31-level voltage and current waveforms. A comprehensive comparative analysis of this new topology was conducted against recently proposed topologies; the results show that the proposed MLI requires fewer components to achieve the desired output compared to other similar topologies. Furthermore, the cost factor per level for the proposed topology is superior. Simulation results reveal that the THD value is 3.73%, indicating good harmonic performance. The proposed topology also complies with IEEE 519 and clarified standards, demonstrating its suitability for practical applications. To verify the effectiveness of the proposed inverter with SPWM and MPPT, a simulation is implemented by utilizing the MATLAB program. As a result, the proposed inverter exhibits several encouraging properties, making it a promising choice for the MLI with PV system applications.

CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

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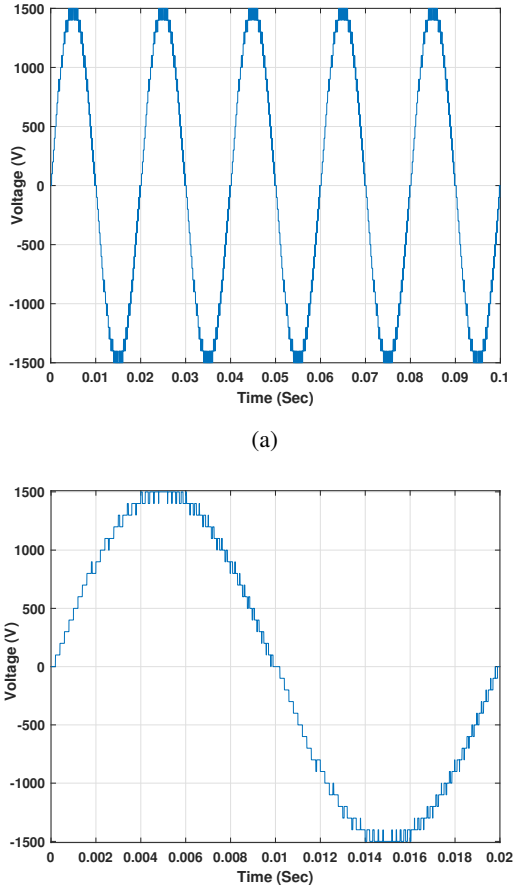

Fig. 12. (a) The output voltage of 31-level MLI at $1000\,W/m^2$ and $25^{\circ}C$ for resistive $R = 100\,\Omega$; (b) Zoom view of Fig.12(a).

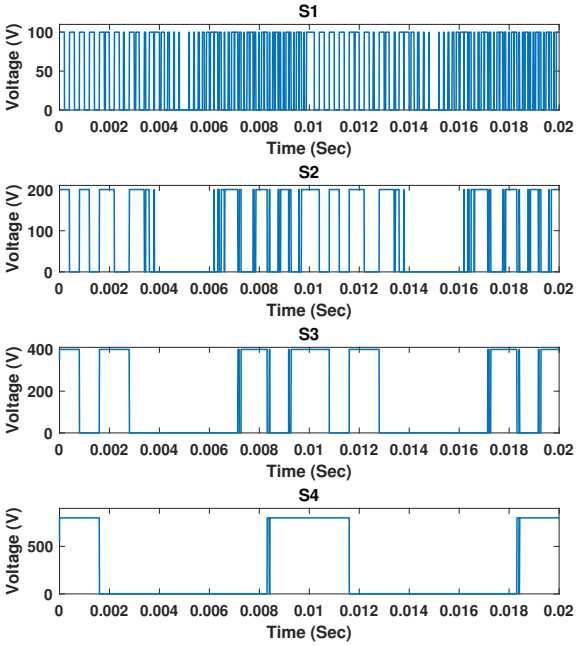

Fig. 13. The voltage waveforms across switches (S1-S4) of MLI for load $R = 100\,\Omega$ at $1000\,W/m^2$ and $25^{\circ}C$.

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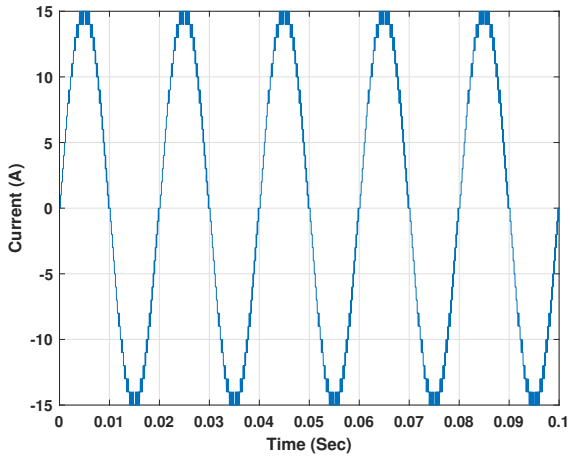

Fig. 14. Output current of 31-level MLI at $1000\,W/m^2$ and $25^{\circ}C$ for load $R = 100\,\Omega$.

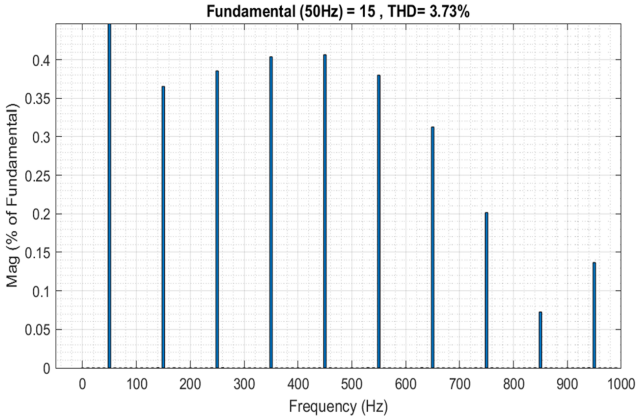

Fig. 15. The THD for voltage and current waveforms are displayed for the 31-level MLI at $1000W/m^2$, $25°C$ and fundamental frequency equal to $50H_Z$.

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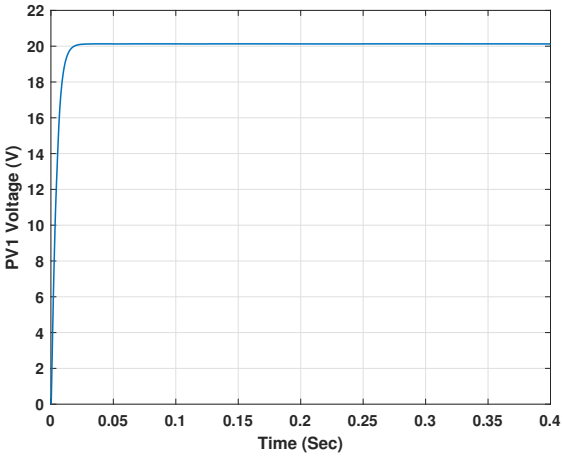
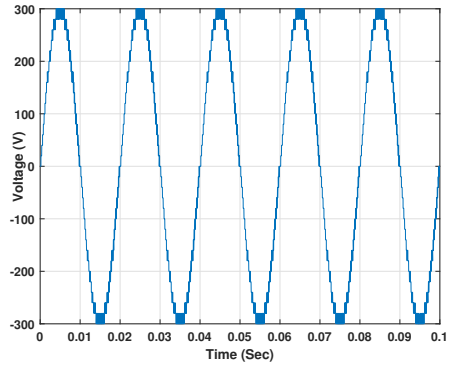
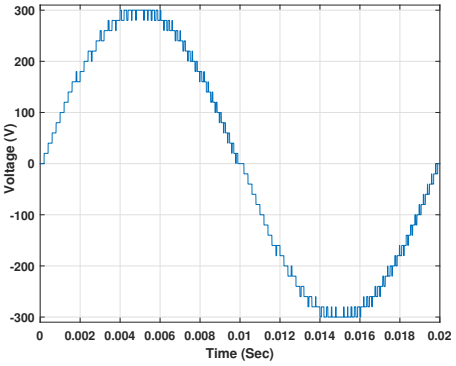


Fig. 16. . Output voltage waveform of PV1 at $200\,W/m^2$ and $25°C$ with boost converter and IC algorithm for resistive $R = 100\,\Omega$.



(a)



(b)

Fig. 17. (a) The output voltage of 31-level MLI at $200\,W/m^2$ and $25°C$ for for resistive $R = 100\,\Omega$ (b) Zoom view of Fig.17(a). .

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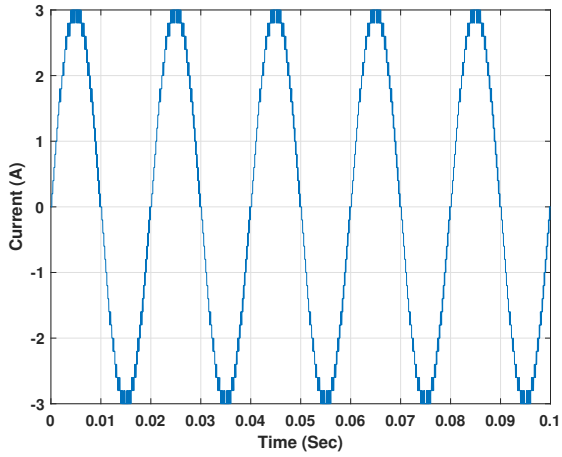

Fig. 18. The output current of 31-level MLI at $200\,W/m^2$ and $25^{\circ}C$ for for resistive $R = 100\,\Omega$.

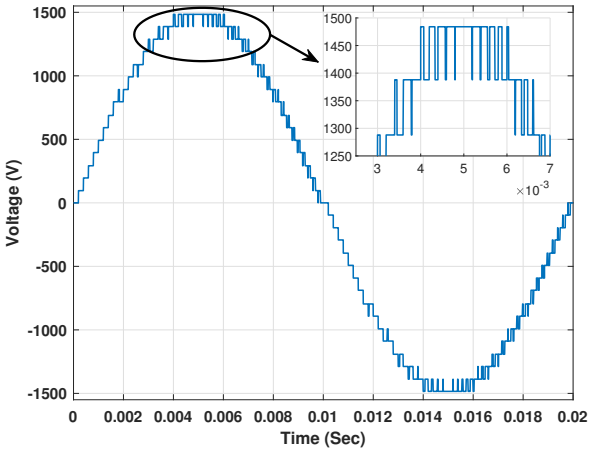

Fig. 20. The output voltage of 31-level MLI at $1000\,W/m^2$ and $40^{\circ}C$ for load $50\,\Omega + 100\,mH$.

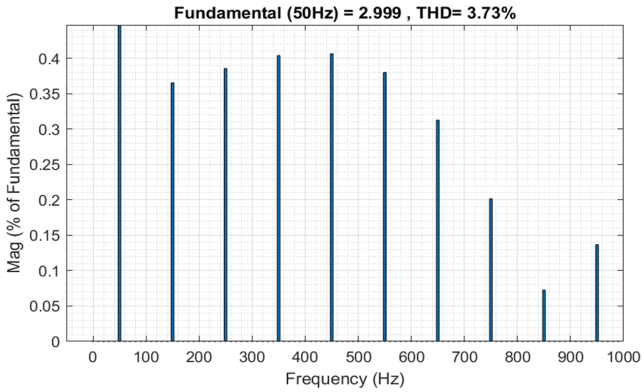

Fig. 19. The THD for voltage and current waveforms are displayed for the 31-level MLI at $200W/m^2$, $25^{\circ}C$ and fundamental frequency equal to $50H_Z$ for resistive $R = 100\,\Omega$.

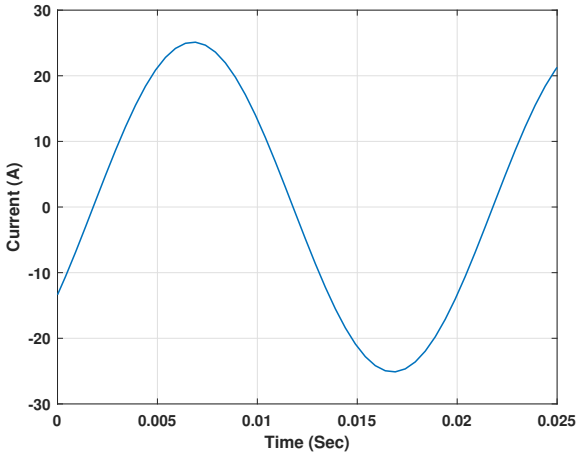

Fig. 21. The output current of 31-level MLI at $1000\,W/m^2$ and temperature $40^{\circ}C$ for load $50\,\Omega + 100\,mH$.

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