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Power Efficient LNA for Satellite Communications

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Abstract
This article presents a power-efficient low noise amplifier (LNA) with high gain and low noise figure (NF) dedicated to satellite communications at a frequency of 435 MHz. LNAs' gain and NF play a significant role in the designs for satellite ground terminals seeking high amplification and maintaining a high signal-to-noise ratio (SNR). The proposed design utilized the transistor (BFP840ESD) to achieve a low NF of 0.459 dB and a high-power gain of 26.149 dB. The study carries out the LNA design procedure, from biasing the transistor, testing its stability at the operation frequency, and finally terminating the appropriate matching networks. In addition to the achieved high gain and low NF, the proposed LNA consumes as low power as only 2 mW.

Keywords
Ground station front end, LNA, Noise figure, Satellite communications, Satellite IoT.

I. Introduction

Currently, existing Internet of Things (IoT) networks offer the interconnection for hundreds of millions of devices worldwide, providing an endless list of convenient daily life applications such as healthcare [1, 2], agriculture [3], and danger detection and alarming [4, 5]. However, these services are not yet inclusive to isolated areas such as oceans, wildwood, deserts, and south and north poles [6]. Thus, future 6G networks seek the engagement of satellites into conventional IoT network towards the aimed global coverage with no topographical limitations creating an emerging new field named satellite IoT (SIoT) [6]. Out of multiple satellite categories, small satellites have gained research attention for such engagement because of their low orbit altitude, the affordable cost to manufacture and launch, and low path degradation losses [7]. In addition, most recently launched satellites are small ones, reflecting an even better opportunity for realistic ubiquitous coverage.

Nevertheless, small satellites are always designed with size and resource restrictions implying low gain transmitting antennas and low power transmitted signal [8]. At the receiver side, the receiving ground terminal will have difficulty retrieving the original data from such received weakened and noisy signals. The ground terminal's operator must then utilize an expensive steerable high gain antenna along with a well-designed low noise amplifier (LNA) [9] . LNAs are vital components of such systems to amplify the received weak signals without adding extra noise [10]. Moreover, achieving signal amplification with very low noise levels allows more accurate and reliable signal detection in successive procedures. Furthermore, the performed high gain LNA helps widen the margin of the link budget calculation at the receiver side.

In the last decade, many designs of LNA structures have been proposed for different applications like, IoT applications [11], magnetic probes [12], and 5G [13]. More relevant LNAs

for satellite communications applications were reported in [14–19] and should be examined in deep in the following paragraph.

In [14], a 3-stage LNA was designed to serve GPS applications at a frequency of 1.57 GHz, achieving a gain of 23.89 dB, a noise figure (NF) of 1.77 dB, and a power consumption of 6.54 mW. 2-stage LNA was reported in [15] for satellite communications at 401.635 MHz resulting in a gain of 28 dB and a relatively high NF of 3.6 dB. Another 2-stage LNA for CubeSats at 29.15 GHz was presented in [16], where the achieved high gain was 39 dB but on the price of high-power consumption of 420 mW and high NF of 2.8 dB. The study conducted in [17] was to design a LNA for CubeSats at 13-14 GHz consuming 162mW of power to generate a gain of 15.5 dB and a NF of 2.4 dB. Serving the same previous application and at the same operation frequency, the study in [18] depicted an LNA design that consumes a higher power of 3.2 W to produce a high gain of 54 dB while maintaining almost the same NF of 2.3 dB. Lastly, the findings of LNA designed for radar, nanosatellites, and GPS applications in [19] revealed a wide-band operation frequency of 0.1-2 GHz with a power gain of 11.3 dB and a high NF of 2.9 dB.

Enlightened by the surveyed LNAs in the literature, this work presents an optimal LNA design for satellite communications ground terminals whose novelty is to achieve a high gain of amplification and yet maintain very low NF. Moreover, the depicted LNA takes into consideration the power consumption efficiency. As for this aimed LNA, the design and simulation were conducted in the environment of AWR Microwave Studio [20]. The rest of this article is organized as follows: Section II describes the LNA design procedure, including the biasing circuit, transistor stability verification, and matching networks. Section III presents the study results and compares findings versus previous designs. Section IV briefly concludes the presented LNA achievements.

II. LNA DESIGN

After selecting (BFP840ESD) transistor for the intended LNA design, the following parts describe in detail the design procedure, including the biasing, stability, and matching networks.

A. Transistor biasing circuit

The biasing circuit of a transistor is necessary to ensure the operation in the active region. Figure 1 demonstrates the biasing network for the transistor after connecting the biasing elements.

For this NPN transistor to function as an amplifier, its emitter-base and collector-base junctions must be forward and reverse-biased, respectively. The datasheet of the selected transistor (BFP840ESD) provides the following specifications:

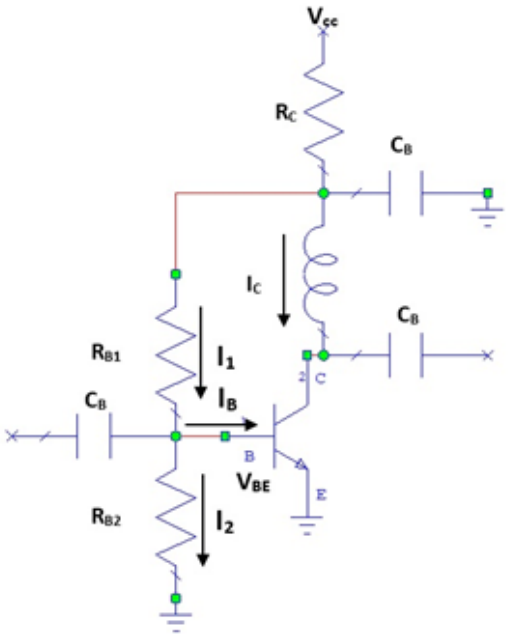

Fig. 1. The biasing network for the transistor (BFP840ESD) to work as an amplifier

The collector current is (Ic= 2 mA), collector-emitter voltage (VCE=1 V), forward base-emitter voltage (VBE=0.8 V), and DC current gain (hFE=250). Assuming the VCC voltage is 1.2 V, the other elements of the biasing circuit are calculated using the well-known biasing equations and listed in Table I.

TABLE I.
RESULTING BIASING CIRCUIT PARAMETERS

Parameter	I_B	R_{B1}	R_{B2}	R_c
Value	8μA	$10K\Omega$	$4.54K\Omega$	$96K\Omega$

B. Transistor stability

The transistor can be either unconditionally stable or potentially unstable based on the magnitude values of input and output reflection coefficients, $|\Gamma_{in}|$ and $|\Gamma_{out}|$. If $|\Gamma_{in}| < 1$and $|\Gamma_{out}| < 1$, the transistor is unconditionally stable. Otherwise, the transistor's stability may oscillate for different loads. The unconditional stability factor (Rollet stability factor or K factor) is a measure of the LNA's stability. It is calculated using the transistor's scattering parameters as in equation (1).

$$K = \frac{(1-|S_{11}|^2+|\Delta S|^2)}{(|S_{12}|^2-|S_{21}|^2)} \quad (1)$$

where, S_{11} is the input reflection coefficient, S_{12} is the reverse transfer parameter, S_{21} is the forward transfer parameter, and

ΔS is the determinant of the reflection coefficients matrix. The stability of the transistor should be examined at the aimed frequency of 435 MHz. The AWR Microwave studio offers two metrics to identify whether the transistor is stable or not. These metrics are the Rollet factor (K factor) and Stability Circle Impedance Ratio (SCIR).

In the Rollet factor linear plot diagram, the transistor must have a value slightly more than 1 at the operation frequency to be stable. On the other hand, the SCIR is calculated by measuring the distance from the center of the Smith chart to the point where the stability circle intersects the unity gain circle. The SCIR is a useful parameter to evaluate the stability of an amplifier design because it provides information about the impedance match between the source and the load. For the transistor to be stable, the curve line must be outside the unity circle in the SCIR polar plot.

After terminating the transistor to the input and output port in AWR Software, as shown in Figure 2 The evaluated K factor and the SCIR were as depicted in Figures 3 and 4, respectively.

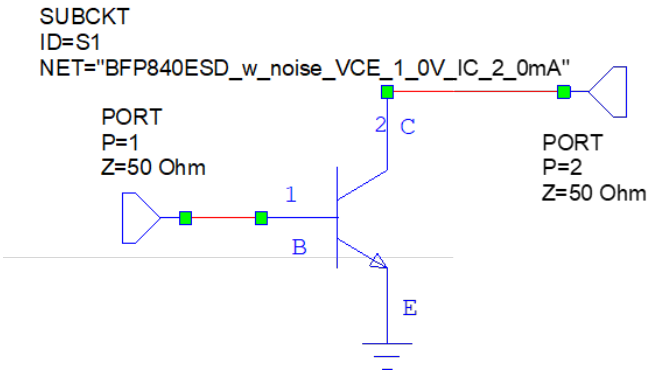

Fig. 2. Initially generated schematic diagram

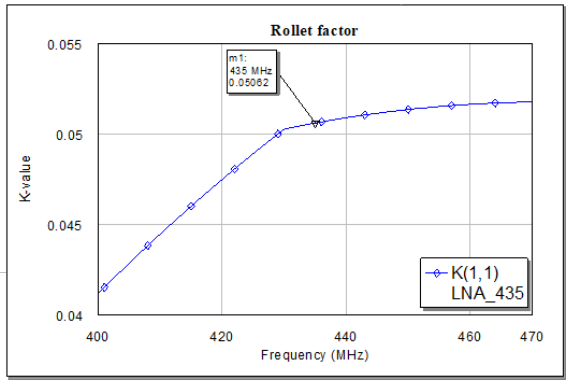

Fig. 3. LNA Rollet factor versus frequency

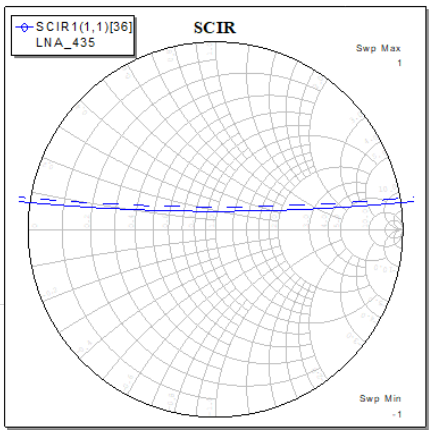

Fig. 4. SCIR polar plot for stability test at 435 MHz

Looking at the simulated results presented in Figures 3 and 4, the Rollet factor has a value of 0.05, while the SCIR curve lies inside the unity circle, implying an unstable transistor at this operation frequency. Thus, a stabilizing method should be involved. The simulation was performed on a range of (400-470) MHz with a resolution of 1 MHz. Thus, the LNA operation frequency of 435 MHz is located at the step (36) as indicated in the legend of Figure 4.

One common method that can be used as a stabilizer is to connect a series or shunt resistor to the transistor collector. In this design, a shunt resistor is utilized with a slider to precisely determine the required value for the transistor to be stable. The slider is slightly increased and decreased while observing the Rollet factor and the SCIR plots. Following this mechanism, the optimal resistor value is 60 Ω.

The stabilizer resistor shunt termination is shown in Figure 5 and the resulting modified Rollet factor and SCIR diagrams are presented in Figures6 and 7, respectively. Figures 6 and 7 show a stable transistor with Rollet factor of slightly more than one and a curve outside the unity circle in the SCIR plot.

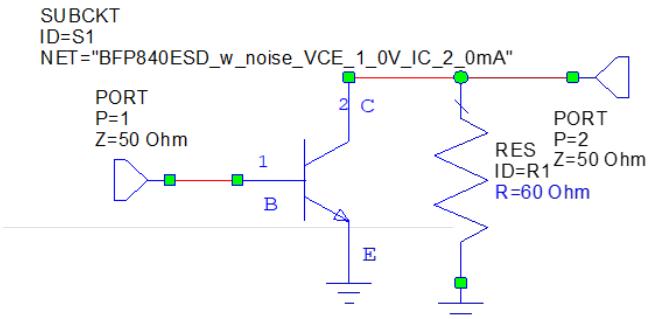

Fig. 5. Modified schematic diagram after terminating the transistor to a shunt stablizer

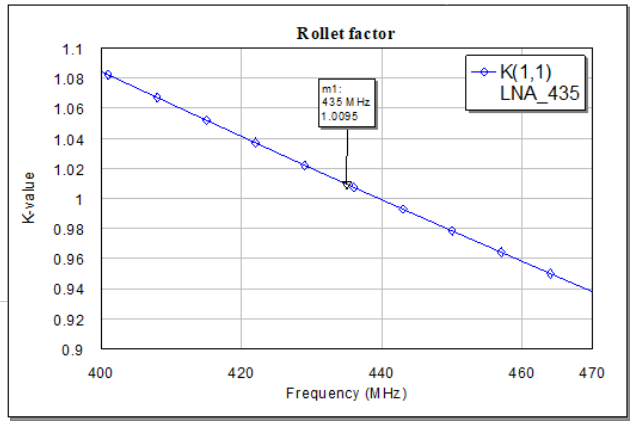

Fig. 6. Rollet factor versus frequency for the stable transisor

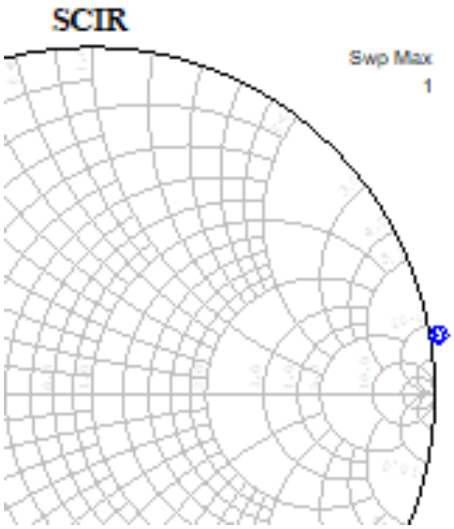

Fig. 7. SCIR polar plot for the stable transistor

C. *Matching networks*

The next step is to evaluate the losses caused by the reflection of the power at the input and output ports. The amount of the reflected power at the input and output ports is relevant to how well-matched these two ports are to the source and the load. The impedance mismatch between the input port and the source results in more reflection of the input power. Similarly, the return losses at the output port are increased when that port is mismatched to the load. Consequently, the impedance mismatching causes the efficiency of the amplifier to reduce. S_{11} and S_{22} parameters indicate how these two ports are well-matched to the source and the load.

Impedance matching is crucial to improve the performance of an LNA by maximizing the power transfer and minimizing the NF through diminishing the losses of impedance mismatch. Furthermore, selecting the right and suitable matching method depends on several criteria. For instance, a simple design with a minimum number of lumped elements is preferred because it is affordable to implement and introduces less losses. Figure 8 demonstrates the matching performance of the transistor at the operation frequency of 435 MHz.

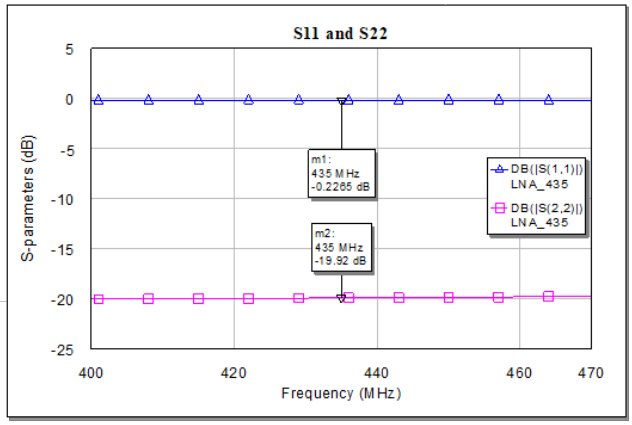

Fig. 8. S-parameters of the stable unmatched LNA

Observing the performance of the transistor in the S_{11} and S_{22} graphs, neither the input nor the output ports are perfectly matched to the source and load terminals. The S_{11} curve indicated a magnitude value of -0.22 dB which implies a complete reflection of the input power at port 1. On the other hand, the S_{22} parameter curve showed a low reflection value of -19.92 dB at port 2. Despite the low value of the reflected power at port 2, the resulting flat S_{22} response also inspires the importance of the matching network for this transistor since such a wide band response may cause more vulnerability to electromagnetic interferences. As a result, the transistor should be terminated to input and output matching networks to provide the aimed performance at the specified frequency.

The input and output matching networks design starts with the evaluation of the current values of the input and output impedance values from the Normalized Frequency Circle Impedance Ratio (NFCIR) and S_{22} polar plots, as presented in Figures 9 and 10.

The NFCIR plot helps visualize and analyze the input impedance characteristics of a circuit over a range of frequencies. By plotting the normalized impedance on a polar graph, it provides insights into the impedance variation and the corresponding stability of the circuit. To evaluate the output impedance matching, the output reflection coefficient S_{22} is used in its polar form. The input impedance from the NFCIR $1.805 + 2.660i$ is taken into Smith chart software after normalized to 50 Ω and conjugated. The resulting impedance of (90-133i) is used in a Smith chart software to evaluate

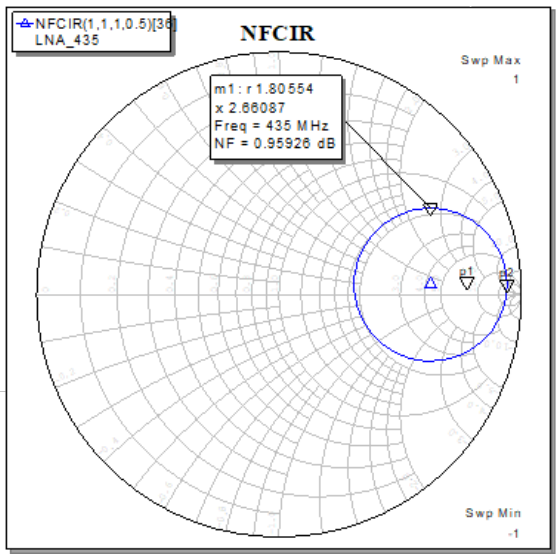

Fig. 9. NFCIR polar plot for evaluating input impedance

the required lumped elements at the input matching network. Similarly, from S_{22} polar plot, we get the output impedance of $1.251 - 0.161i$, which becomes $62.55 - 8.05i$ after normalized to 50 Ω. The schematic diagram in Figure 11 shows the input and output matched transistor with the calculated lumped elements.

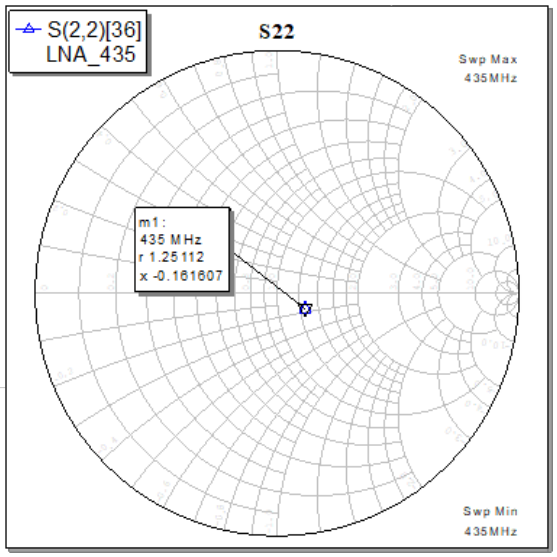

Fig. 10. S22 polar plot for evaluating output impedance

The performance of the transistor after the matching networks design is again observed through the S_{11} and S_{22} parameters and presented in Figure 12.

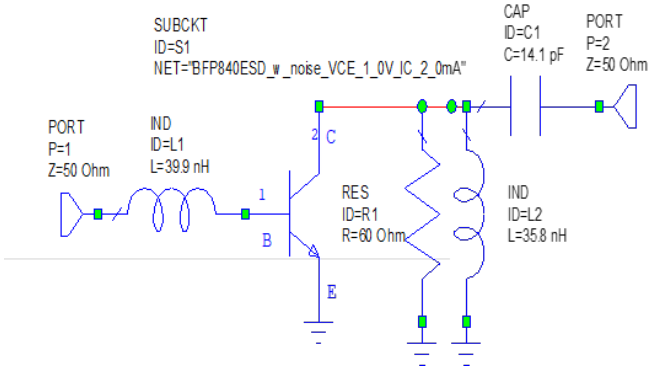

Fig. 11. Modified schematic of the matched stable transistor

The S_{11} and S_{22} curves in Figure 12 are not yet promising enough for the transistor to meet the requirements of the LNAs for small satellites. Figure 12 shows an input reflection coefficient of -0.32 dB which emphasis the almost total reflection of the input power at the input port. On the other hand, the resulting reflection coefficient at the output port indicated the perfect matching of that port to the terminated load.

Thus, the lumped elements were optimized using the AWR optimizer algorithm of Particle Swarm. Particle Swarm is a well-known optimization algorithm that can be used to find optimal values of several variables after setting certain goals to meet. This algorithm is a built-in option in AWR and was used to evaluate the optimal values of the lumped elements to achieve the requires S_{11} and S_{22} goals of (< -10) and (< -40), respectively. These introduced goals must be met within the frequency range of (430-440) MHz which represents a ±5 MHz around the operation frequency of 435 MHz.

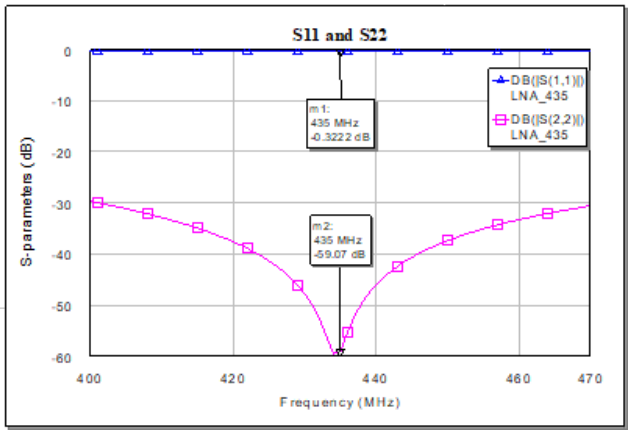

Fig. 12. S-parameters after terminating matching networks

The optimized lumped elements are terminated to the transistor as in Figure 13. The optimized lumped elements were

standardized to realizable values according to the market availability. The depicted values of the lumped elements in Figure 13 achieved the given gaols of $S_{22} < -40$ and $S_{11} < -10$ for the ±5 MHz around the operation frequency of 435 MHz.

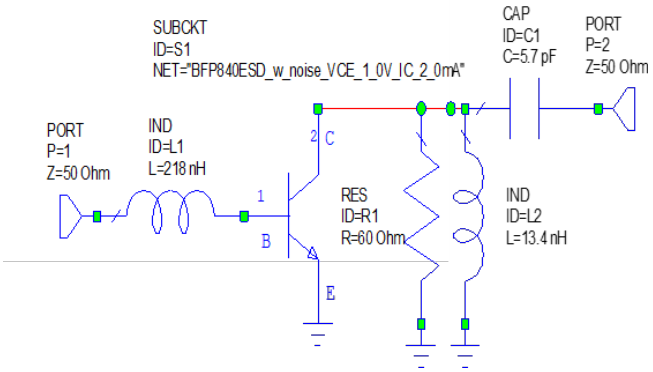

Fig. 13. LNA schematic diagram with optimized lumped elements

III. RESULTS

The input and output-matched transistor performance results are presented in terms of the S-parameters, the power gain, and the NF. In Figure 14, the S_{11} and S_{22} parameters show good magnitude values that satisfy the satellite communications design requirements. Furthermore, the designed LNA offers a power gain of about 26.149 dB at 435 MHz, as demonstrated in Figure 15. The proposed LNA achieved a low NF value of 0.459 at the targeted operation frequency,as presented in Figure 16. The achieved high gain along with the very low NF were not at the price of design complexity since the depicted LNA design is a single stage amplifier with proper biasing and matching networks.

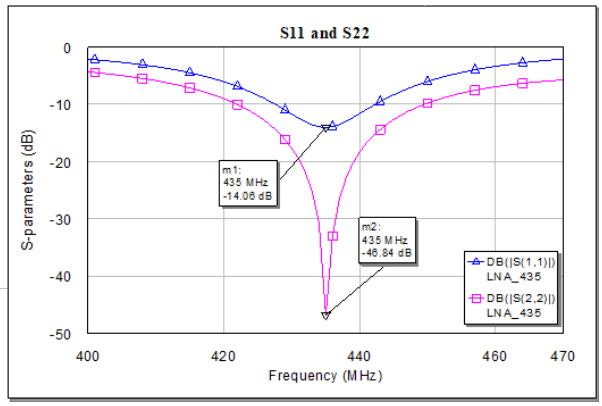

Fig. 14. S-parameters of the optimized LNA

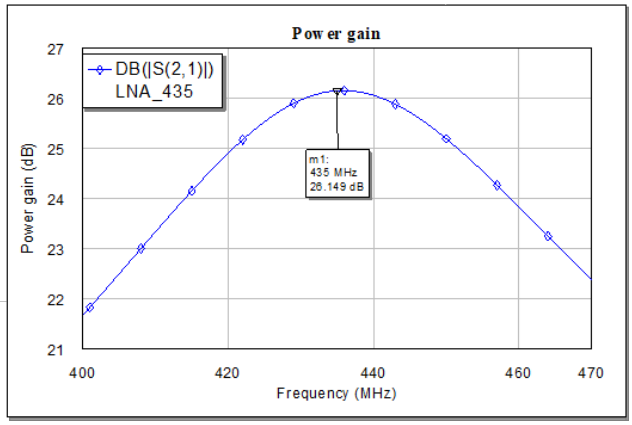

Fig. 15. Optimized LNA's Power gain

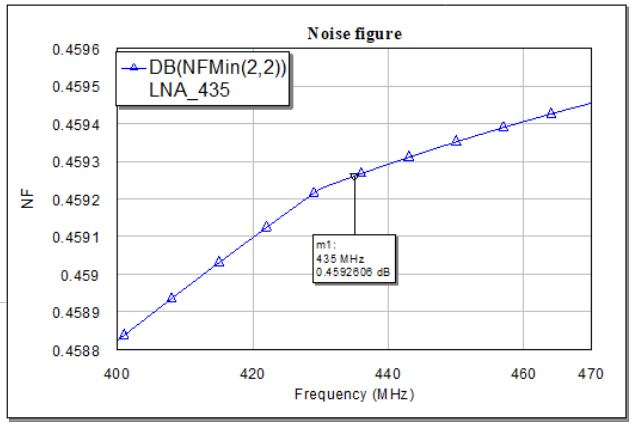

Fig. 16. NF versus frequency for the optimized LNA

Further insight into other achievements from the literature versus the findings of the presented work are compared in Table II. Throughout this comparison table, we can clearly see how the listed previous designs were subject to the tradeoff to either achieve good gain at the price of poor NF values or vice versa. Even when the previous LNAs achieved high gain and an acceptable noise figure, they lacked consideration regarding power consumption. This study offered an LNA design capable of achieving high gain at a very low NF and consuming considerably low power.

These achievements emphasis the novelty of this design to not only fulfill the aspirations of the satellite communications requirements but also meet the aim of constructing affordable and simple amateur ground stations for small satellites.

TABLE II.
COMPARISON OF THE PROPOSED WORK WITH PREVIOUS LITERATURE

Specifications	[15]	[19]	[21]	[22]	[23]	[24]	[25]	This work
Frequency (GHz)	0.401	$0.1-2$	$0.1-1.45$	$0.2-1.6$	$0.13-0.93$	$0.1-1$	0.434	0.435
Supply voltage (V)	1.08	9	1.8	1.2	1.8	1.2	3.3	1.2
Consumed power (mW)	6.5	-	9.5	0.7-3.1	3	2.7	-	2
Gain (dB)	28	11.3	16.9	6.2-8.8	16.6-19.6	14	16.5	26.149
Noise figure (dB)	3.6	2.8	2.5	2.31-3.68	3.6-5e	4	0.63	0.459
Input return loss (dB)	-16.4	-8.9	-17	-20	<-10	<-10	-2.6	-14.06
Output return loss (dB)	-18.7	-	-15	-	-	-	-16.4	-46.84
Applications	Sat. Comm.	GPS	Wideband receiver	-	IoT	Wireless communication	Sat. Comm.	Sat. Comm.

IV. CONCLUSIONS

In summary, the proposed LNA design can serve satellite communications applications at the amateur's frequency of 435 MHz. The findings of the simulated LNA revealed a high gain of 26.149 dB while maintaining a very low NF of 0.459 dB. Besides the high gain and low NF, the presented LNA only consumes 2 mW of power when supplied by 1.2 V. These promising findings come along with 14.06 and -46.84 dBs for the input and output return losses, respectively. Such LNA enables the ground station terminal to receive, process, and decode the weak signals transmitted by small satellites when engaged in future SIoT networks. More promising results at the ground station terminal are assured if this LNA is confronted by a well-designed band-pass filter, which prevents the LNA from being overdriven by the received broad power spectrum.

CONFLICT OF INTEREST

The authors of this article hereby declare no conflict of interest. They have read and reviewed the manuscript and agreed on the publication as open access material.

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