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# Comparison of New Multilevel Inverter Topology with Conventional Topologies Used for Induction Heating System

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**Abstract**

***In this article, a comparison of innovative multilevel inverter topology with standard topologies has been conducted. The proposed single phase five level inverter topology has been used for induction heating system. This suggested design generates five voltage levels with a fewer number of power switches. This reduction in number of switches decreases the switching losses and the number of driving circuits and reduce the complexity of control circuit. It also reduces the cost and size for the filter used. Analysis and comparison has been done among the conventional topologies (neutral clamped and cascade H-bridge multilevel inverters) with the proposed inverter topology. The analysis includes the total harmonic distortion THD, efficiency and overall performance of the inverter systems. The simulation and analysis have been done using MATLAB/ SIMULINK. The results show good performance for the proposed topology in comparison with the conventional topologies.***

**KEYWORDS: Multilevel inverter (MLI), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM), Induction Heating (IH).**

## I. INTRODUCTION

Multilevel inverter MLI is a power electronic converter device used to generate high number of voltage levels. It's used in medium and high voltage application [1].
The significance of multilevel inverters is associated with their power quality, harmonic amplitude reduction, and capability to generate as near to a sine wave output voltage as possible.

Because of their ability to provide a high quality voltage waveform and reduced current and voltage rating of the used switches, multilevel inverter topologies have seen significant growth in industrial applications in recent years [2].The primary types of multilevel inverters are diode or neutral clamped point multi-level inverter, cascaded H-bridge multilevel inverter and flying capacitor multilevel inverter [3].

New inverter topologies have been proposed by many researches that aim to improve the quality of the energy available at the inverter terminals [4].

In (2012) M. R. Banaei, H. Khounjahan, and E. Salary introduced multilevel inverter topology which was the cascaded transformer inverter. That topology consisted of single DC source and numerous single phase transformers to create three levels using two switches as compared with conventional one which requires four switches, and all transformers need just two switches to change the direction of a single DC source. The experimental results demonstrated that the suggested architecture can provide high quality output voltages, but the primary drawback of that topology was the need of switches with high current rating than traditional topology. Despite the fact that the usage of transformers make the inverters design more complex and expense [5].

Another cascade multi-level inverter proposed in [6]. That inverter composed of series connection of cells (each cell consist of 3 DC voltage sources and 5 switches) which produced positive levels and full bridge was included to produce negative output levels. Four distinct algorithms had been presented to identify the magnitude of DC sources in order to produce all voltage levels (even and odd) at the output of the proposed topology. That inverter topology required fewer power electronic equipment, resulting in less cost of the inverter. The experimental findings were validated using 15-level inverter. The major drawback of that

inverter was the need for many separate DC sources to supply the inverter.

In (2014), R. Nagarajan and M. Saravanan developed a 9 level cascaded multilevel inverter with reduced switching components, carrier signals and gate drivers. It included hybrid structure of two portions, the first one generate the level voltage using high-frequency switches. The other part generate the polarity of the output voltage using low frequency switches. That topology required eleven switches and four separated sources are required. The findings clearly indicated that the suggested architecture might function as a multilayer inverter with fewer switches and carriers [7].

In (2015), N. Prabaharan and K. Palanisamy investigated 15 level inverter with asymmetric DC source and different types of multicarrier PWM signals. Comparison had been done among the suggested reduced switches topology and the classical topologies (Diode clamped, Flying Capacitor and Cascade H-Bridge). The suggested configuration consisted of eight switches (two of them were connecting with DC sources), that arrangement had been utilized to double the output level of voltage based on the values of DC sources [8].

V. Rajkumar and T. Nadu introduced a model of a 21-asymmetric cascade MLI with a lower number of switches. The inverter used in that study employs just 11 switches, 3 diodes, and 4 asymmetrical sources with multicarrier PWM to generate the required output voltage. For the reverse current flow problem, anti-parallel diodes utilized, allowing several levels to be achieved at the outputs. The simulation shows that even if one of the switches fails, the system can still produce numerous voltage levels without shunting down the entire system. The used topology in this study employs a lower number of power semiconductor components and minimizes overall cost [9].

A. I. M. Ali et al. created an arrangement for a single-phase, five-level inverter with load voltage control via PWM in (2018).The basic construction of that inverter consists of two parts. The first one is a full H-bridge inverter, which is responsible for the polarity of the output voltage. The second part (consisting of two cells) is responsible for adjusting the output level of voltage. The two cells connected in series. The first one contains a single DC-source in series with a switch, and this series combination connected in parallel with the diode, while the second one consists only of a DC source. A PI controller utilized in a closed loop circuit to manage and regulate sinusoidal load voltage. Even though the developed arrangement used fewer switches and lower harmonic content, the experimental results show lower efficiency than expected [10].

In a separate study [11], two topologies for multilevel output voltage inverters were presented. The first configuration synthesizes (15 levels) at the output. It consisted of three DC voltage sources and ten unidirectional and bidirectional switches. The second configuration consisted of four DC voltage sources and 12 switches to create 25 levels at the output, which is an expansion of the first topology. Both topologies implemented with lower voltage rated across the switches. The experimental findings demonstrate the feasibility of these topologies with various types of loading combinations and various modulation indexes. Even though the two topologies required fewer number of switches, the drawback is the needed to separated DC voltage supplies which increase the inverters cost.

In (2020), V. Anand and V. Singh created a modular inverter with a basic unit that can be extended in series to achieve the required output level voltage. The designed basic unit consisted of four bidirectional and unidirectional switches, and two DC sources. To create a symmetrical 7-level inverter, nine unidirectional and bidirectional switches, and three DC voltage sources are required. Using the same components, it can be generates 15 level with asymmetrical DC voltage sources. When two basic unit connected in series, a maximum of 27 level were formed. Comparison had been made for the developed inverter using five algorithms for asymmetrical multilevel inverter in term of the number of DC sources, stresses on each switch and efficiency. As a result, the developed modular inverter employed fewer ON-state switches and has a lower block voltage across switches. The drawback of that configuration is that the efficiency decreases as the over and under modulation as RMS as well as THD both increases [12].

In (2021), M. S. Bin Arif et al. suggested basic module which operated with symmetrical and asymmetrical DC sources using nearest level control technique. It can generate 15 level at the output with eight switches, and 4 DC sources and it can be generalized to generate more number of levels. When compared with the basic topology, which requires ten switches to produce the same output level voltage. Analysis reveals that the suggested system required lower rated switches and overall block voltage. The findings were achieved for unity power factor loads, as well as with changing modulation index. The results show that with the increasing in output power rating, the efficiency of the designed 15-level inverter reduced [13].

B. Hosseini Montazer, J. Olamaei, M. Hosseinpour, and B. Mozafari, introduced the bidirectional MLI topology to feed low power factor RL loads with symmetrical and asymmetrical DC sources. In the symmetric topology, the suggested unit includes 5 separate DC sources with 9 unidirectional switches, 2 bidirectional switches, and 2 diodes that may yield 11 levels, while the conventional architectures require 12 switches or more to create 11 levels at the output. The asymmetric topology generates 19 levels in the output using the same components. The problem of reverse current and voltage spikes had been studied. The suggested topology analysis has been validated by the experimental laboratory results [14].

In (2021), A. Abdali, A. Abdulabbas, and H. Nekad conducted a comparison between conventional and non-conventional topologies. The non-conventional topologies used in the study were 3-phase 9 and 17 output voltage levels. The 9-levels topology required (11 switches/ phase) and 4 DC sources, while the 17-levels topology required (32 switches/phase) and 8 DC sources. The developed topologies require fewer switches to produce the same output voltage level using the conventional topologies and can be extended to produce a high number of levels [15].

The next section will take an overview about the concept of multilevel inverter and discuss the conventional topologies characteristics, their advantages and disadvantages. Section III will discuss the modulation techniques used to control the inverter switches turning on and off. In section IV, details description about the proposed topology, it's configuration and operation mode. While section V include the MATLAB simulation for the system and the obtaining results from it. Finally, section VI include the final conclusion from this comparison work.

## II. Multilevel Inverter Concept

The aim of multilevel inverters is to create a smoother stepped of waveform of an AC signal with reduced dv/dt and harmonic distortion when compared to conventional two level inverters. The importance of multilevel inverter manifested in reducing the harmonic distortion for some application needed this feature in output voltage. This feature cannot be reached when using two level inverter.

The multilevel concept of inverters had been introduced in the year 1975 to overcome the drawbacks in industrial application inverters like lower efficiency, high cost and switching losses. This inverter concept starts with three levels. Multilevel inverter can deliver AC voltage waveform by using many DC voltage configuration [16].

The output waveform of multilevel inverter takes the form of stair case whose fundamental component is a sinusoidal. There are two categories of inverters used in power application; voltage source inverters and current source inverters.

For multilevel topologies, the VSI has advantages such as the reduction in dv/dt, harmonics, electromagnetic interferences and filter size [17]. The major three topologies of voltage source inverter are the diode or neutral clamped point inverter, flying capacitor clamped multilevel inverter and finally the cascaded H-bridge multilevel inverter.

Neutral clamped multilevel inverter as a compare with other topologies has some advantage like when higher number of output level achieved, harmonic will be low. The main structure of this type is shown in Fig. 1.
The main drawback is that as the output voltage level number rises, the clamping diode is used excessively, making it hard to manage the real power flow of the individual inverter in a multi-inverter system [18].

Cascaded H-bridge (CHB) is another topology which also called cascaded multilevel inverter, no diodes or capacitors used in this topology. The CHB topology consist of number of bridge cells and when used in modular DC/AC inverter, the inverter system will be more reliable. The DC voltage sources are separated in this topology as illustrate in Fig. 2 and increases proportionally with number of produced output voltage level which is the major disadvantage of this multilevel inverter topology [19].

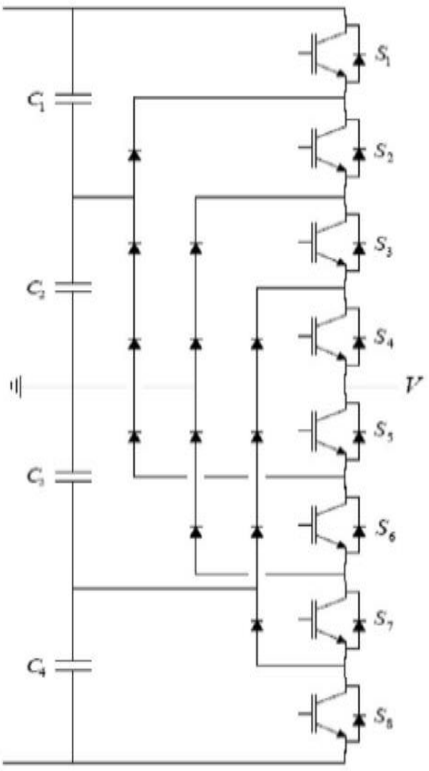



Fig. 1: Structure of diode clamped multilevel inverter.

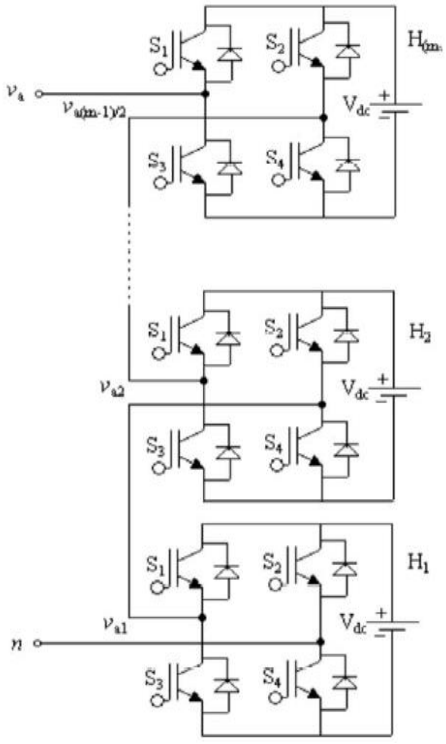



Fig. 2: Structure of cascaded multilevel inverter

The third form of multilevel inverter is the capacitor clamped multilevel inverter illustrated in Fig. 3, also known as a fly-wheel capacitor inverter .The primary distinction between the two topologies, capacitor clamped and a diode clamped multilevel inverter is that the diode is replaced with a capacitor in the capacitor clamped multilevel inverter. To generate an n-level staircase output voltage, the number of capacitors needed is (n-1). A number of supplemental capacitors are added and clamped across switches in a ladder construction, so that each capacitor branch carries a distinct voltage value, which allows mathematical exploitation of the output voltage [20]. The major disadvantage in this topology is large number of capacitors is required when output voltage level is high also the complexity in the inverter control [21].

In general, the only drawback of a multilevel inverter is the need for a large number of switches to produce a variety of voltage levels number. This increment in the number of switches leads to increase the complexity of controlling method and high cost. The suggested topology employs a low number of power switches, which not only reduces the number of driving circuits but also results in excellent efficiency.

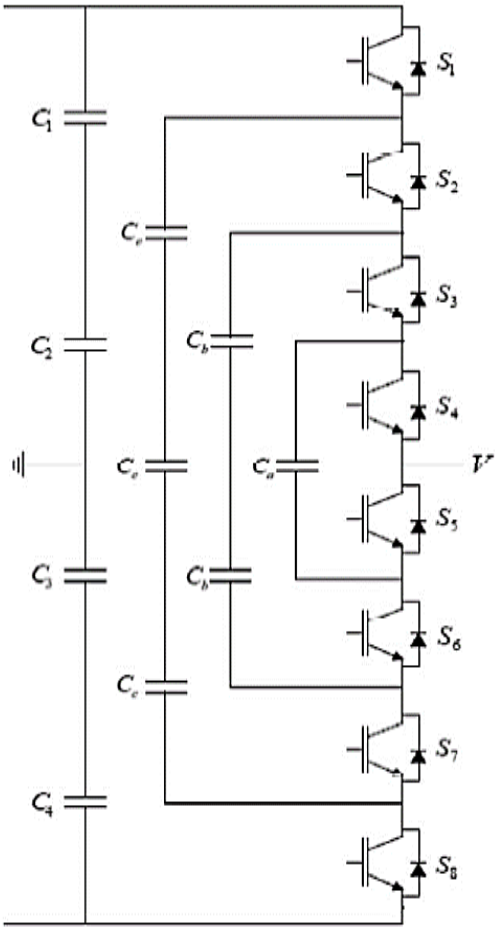



Fig.3: Structure of flying capacitor multilevel inverter

## III. Types Of Modulation Technique

The modulation techniques play an important rule for multilevel inverter since they are directly related to the overall efficiency of the system. Many modulation methods have been introduced for multilevel inverter. For multilevel inverters, modulation methods and control paradigms like sine PWM, selective harmonic elimination and space vector modulation have been developed [22].

Controlling the output voltage and current may be accomplished using modulation methods. The modulation signal's primary aim in MLI is to generate a stepped waveform that is closely similar to the reference signal, which is typically sinusoidal. To achieve a sinusoidal waveform, modulation techniques are categorize into three types: amplitude, frequency, and fundamental component modulation [23].

The multicarrier PWM methods has been utilized in this present work. These methods can be divide in to two types, phase shift and level shift. Phase Shift modulation is a multicarrier modulation method in which all carrier waves are phase shifted from one another. The number of voltage level relates to the number of carriers. All carriers must have similar frequency and peak-to-peak amplitude.

The level shift multicarrier modulation method have the same relation between voltage levels and carriers number as phase shift. This technique differs from phase shift in the disposition of the triangular carriers [24].

The level shift can be subdivide into three subcategories according to the carriers' phase disposition, Inverted phase disposition, phase opposition disposition and alternative phase opposition disposition. In this paper, we focused on these techniques and compared among them for the proposed five level inverter and the two conventional MLI topologies.

## IV. Proposed Topology

The suggested five-level inverter topology is a combined of two conventional topologies, the cascade H-bridge and neutral point clamped multilevel inverter. The suggested five-level inverter's circuit schematic is illustrated in Fig. 4. It is made up of six MOSFET switching devices designated as (SW1, SW2... SW6) and two power diodes designated as (D1 and D2). Two identical capacitors (C1 and C2) has been used to divide the input DC voltage source by connecting them in parallel with the source. Through the two MOSFET switches (SW1 and SW2) and the two power diodes (D1 and D2), the divided voltage transferred to the H-bridge.

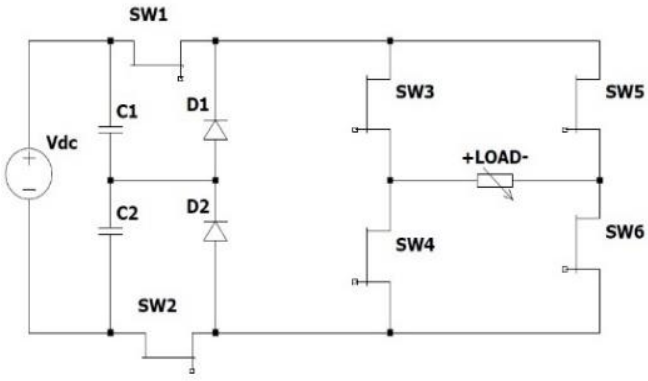



Fig.4: Proposed five level inverter

TABLE I
SWITCHING STATE OF PROPOSED FIVE-LEVEL INVERTER TOPOLOGY.

| SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | Vout |
|---|---|---|---|---|---|---|
| ON | ON | ON | OFF | OFF | ON | +Vdc |
| ON | OFF | ON | OFF | OFF | ON | +1/2Vdc |
| OFF | OFF | ON | OFF | ON | OFF | 0 |
| Off | ON | OFF | ON | ON | OFF | -1/2 Vdc |
| ON | ON | OFF | ON | ON | OFF | -Vdc |

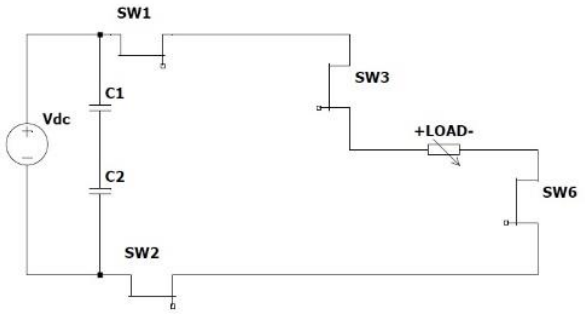
The switching arrangement at various output voltage levels is indicated in Fig. 5.

The operation modes can be describe based on the present path for the switches operation sequence at each mode and it can be stated as follows:

1- Mode 1:

When the two MOSFET (SW1 and SW2) are turned on, the output voltage level Vo=+Vdc, while H-bridge is provided by energy from the DC voltage source. Furthermore, the voltage across the H-bridge is +Vdc.

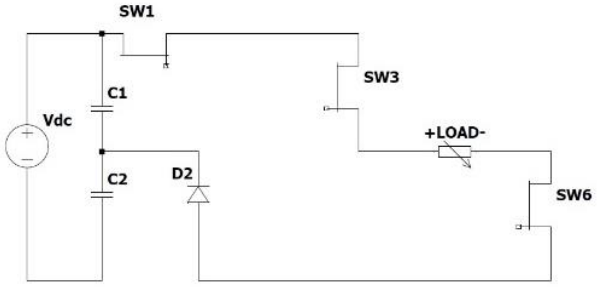
The MOSFET switches SW3 and SW6 are then activated, and the voltage supplied to the load is +Vdc, as illustrated in Fig.5a.




(a)

2- Mode 2:

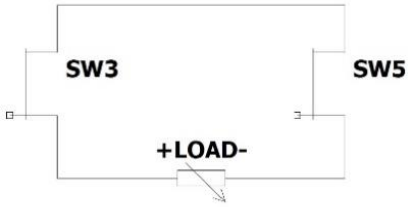
When the diode D2 and MOSFET SW1 are turned on the output voltage level Vo=+1/2Vdc. In this configuration, the H-bridge is connected in parallel with the capacitors (C1). Furthermore, the voltage across the H-bridge is +1/2Vdc. The MOSFET switches SW3 and SW6 are then activated, and the voltage supplied to the load is +1/2 Vdc, as illustrated in Fig. 5b.




(b)

3- Mode 3:

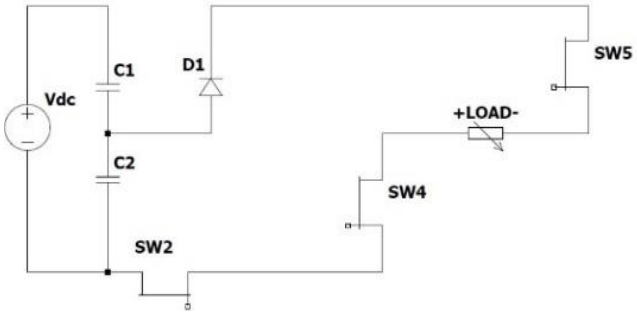
When the two MOSFET (SW3 and SW5) are turned on, the output voltage level becomes zero, and the voltage supplied across the load terminals is Vdc=0, as illustrated in Fig. 5c.




(c)

4- Mode 4:

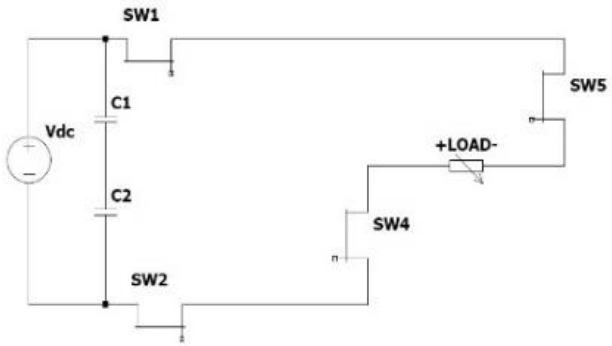
At negative half cycle, the MOSFET SW2 and diode D1 and are turned on the output voltage level -1/2Vdc. In this configuration, the H-bridge is connected in parallel with the capacitors (C2). Furthermore, the voltage across the H-bridge is -1/2Vdc. The MOSFET switches SW4 and SW5 are then activated, and the voltage supplied to the load is -1/2 Vdc, as illustrated in Fig. 5d.




(d)

5- Mode 5:

When the two MOSFET (SW1 and SW2) are turned on, the output voltage level Vo = -Vdc, while H-bridge is provided by energy from the DC voltage. Furthermore, the voltage across the H-bridge is -Vdc. The MOSFET switches SW4 and SW5 are then activated, and the voltage supplied to the load is -Vdc, as illustrated in Fig. 5e.




(e)

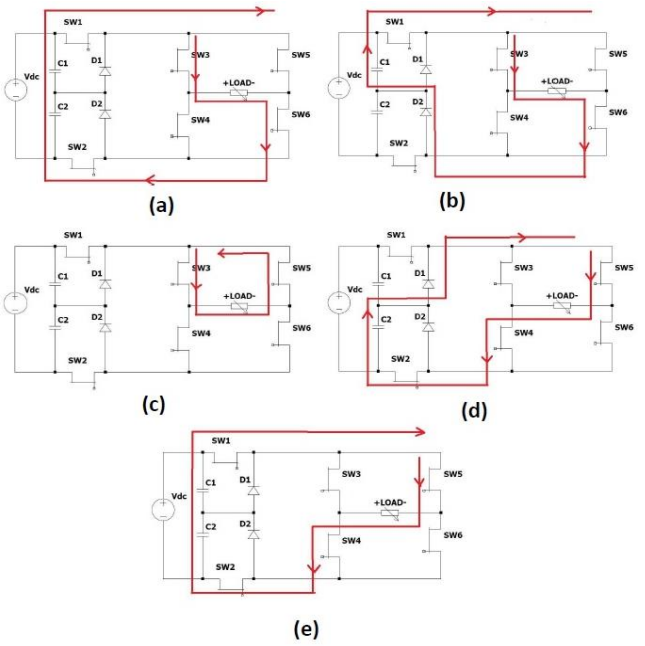
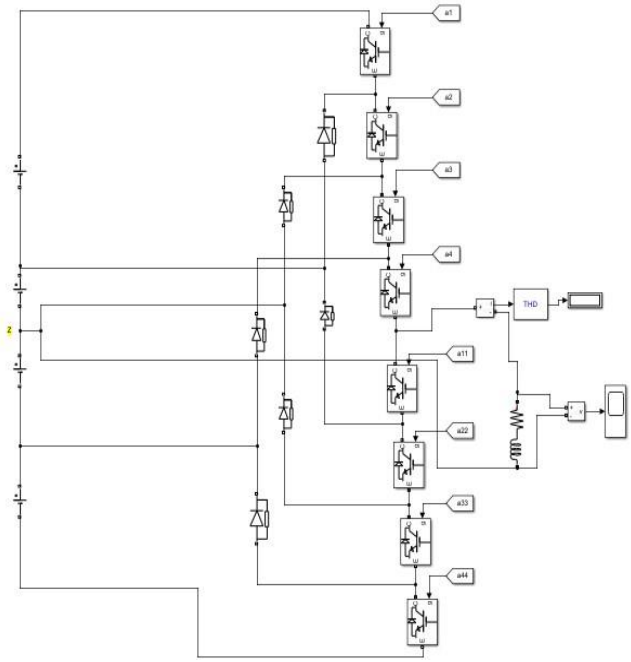


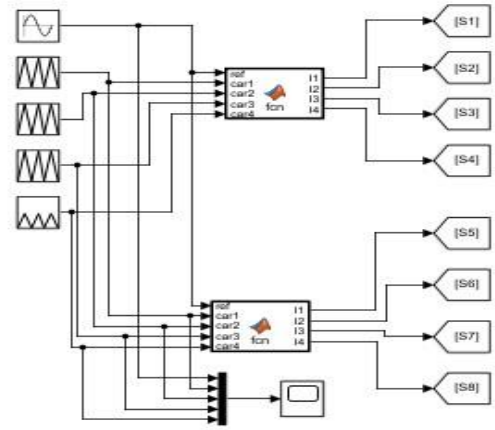

Fig.5: Operation modes of proposed five-level inverter (a) Mode 1 (Vout=+Vdc) (b) Mode 2 (Vout)=+1/2Vdc (c) Mode 3 (Vout= 0) (d) Mode 4 (Vout= -1/2Vdc) (e) Mode 5 (Vout= -Vdc).

## V. Design, Simulation And Results

In this study, MATLAB/Simulink is utilized to simulate the two conventional multilevel inverter topologies which are the neutral point clamped and cascade H-bridge multilevel inverters as illustrate in Figs. 6 and 7 respectively. The proposed five level inverter has been simulated in MATLAB/Simulink as illustrated in Fig. 8.

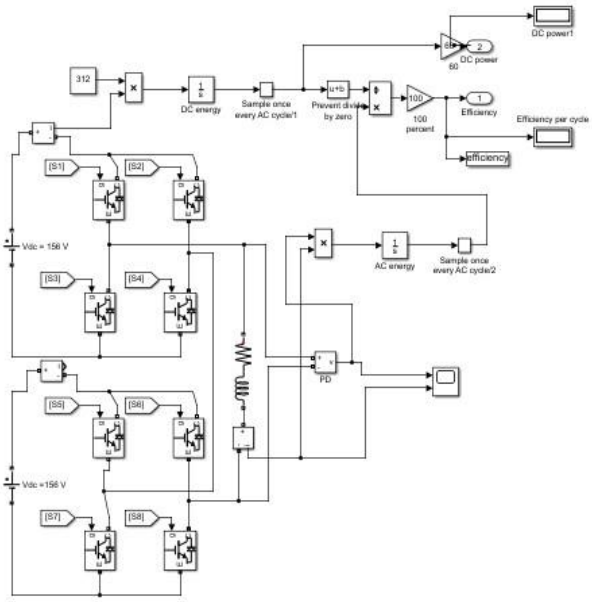



(a)

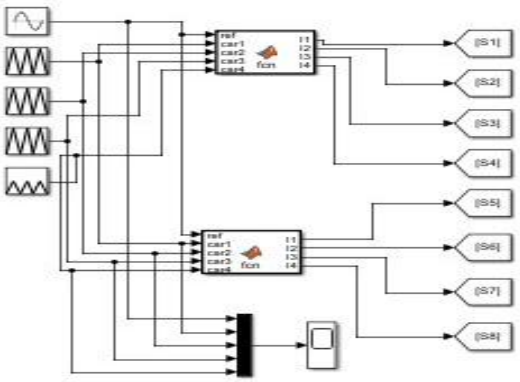



(b)

Fig.6: (a) NC-MLI (b) PWM control.

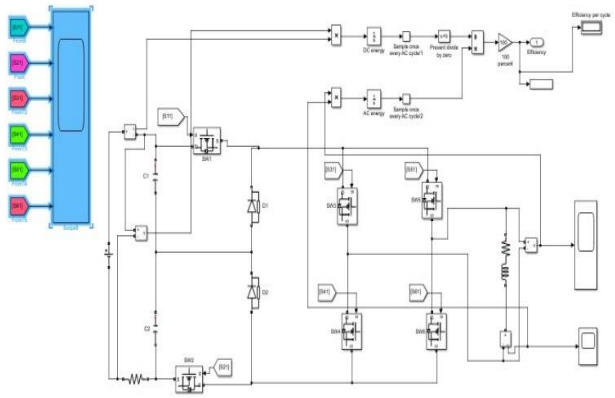



(a)

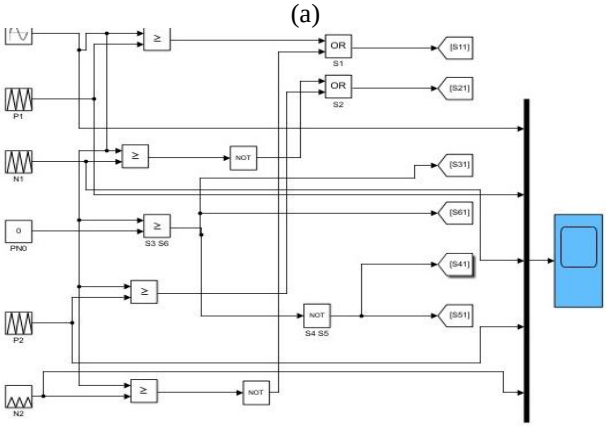



(b)

Fig.7: (a) CHB-MLI (b) PWM control



(a)

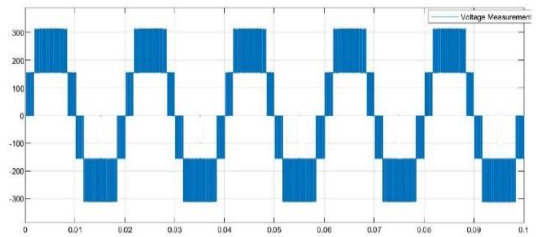



(b)

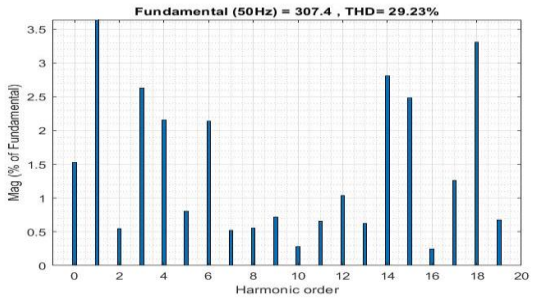
Fig.8: (a) Proposed five level inverter topology
(b) PWM control

The comparison and analysis has been made among those three topologies in terms of total harmonic distortion THD, efficiency and RMS voltage obtained using different technique of level shift PWM.

The output voltage waveform and the total harmonic distortion for the conventional cascade H-bridge multilevel inverter is shown in Fig. 9.



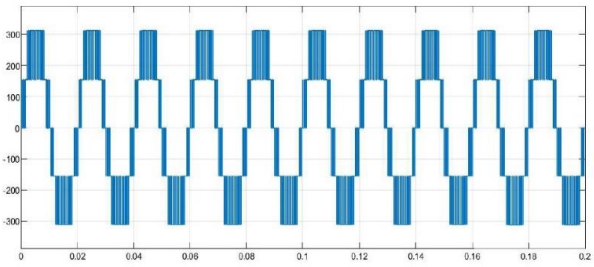
(a)



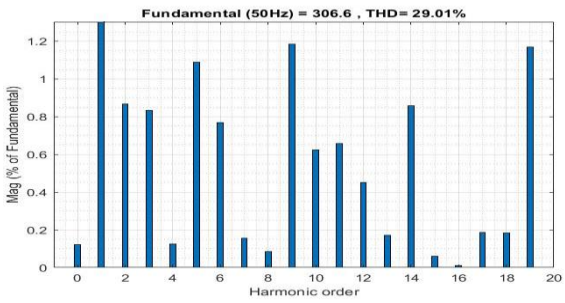

(b)

Fig. 9: (a) Output voltage waveform for CHB (b) THD for CHB

The output voltage waveform and the total harmonic distortion for the conventional neutral clamped multilevel inverter is illustrate in Fig. 10.



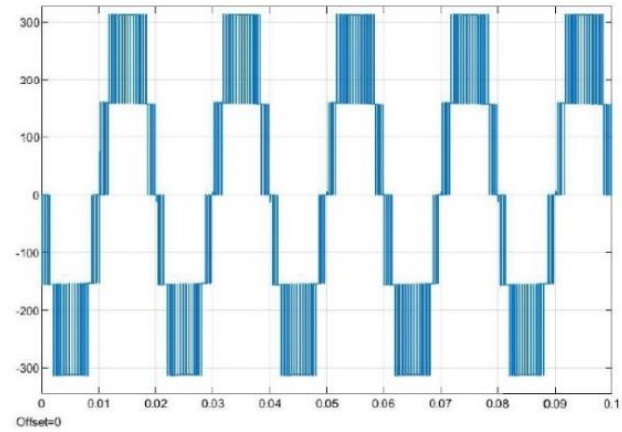
(a)




(b)

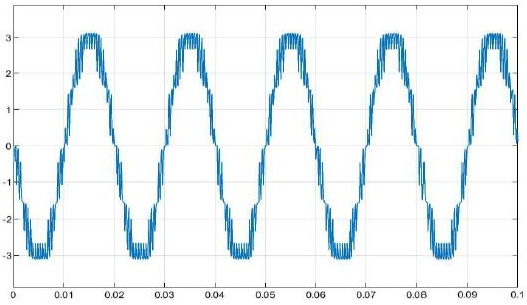
Fig.10: (a) Output voltage waveform for NCI (b) THD for NCI

The simulation results for the two conventional multilevel inverter topologies shows that the total harmonic distortion for the cascade H-bridge multilevel inverter value is 29.23% while the THD for the neutral clamped multilevel inverter is 29.01%. The PWM technique used in these two topologies is phase disposition (PD) modulation technique.
Fig. 11 illustrates the simulation results for the proposed five-level. As can be observed, the suggested five level multi-level inverter has the THD (29.47%) while the THD for CHB and NCI MLI are (29.23% and 29.01%) respectively, which is almost close. To reduce the harmonics for the proposed topology, it's recommend to use low pass filter.




(a)

Fig. 11: Results of proposed five level MLI
(a) Output voltage waveform (b) Output current waveform (c) switching gate pulses (d) four carrier signal (e) THD.



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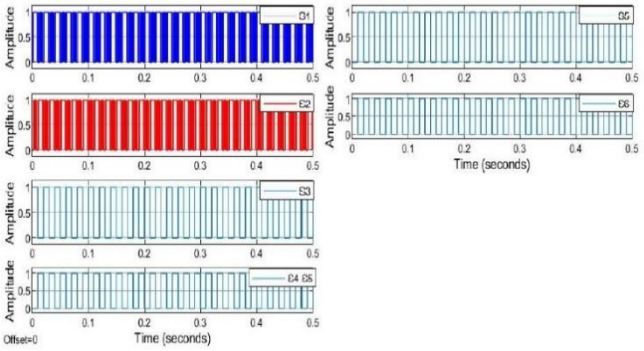
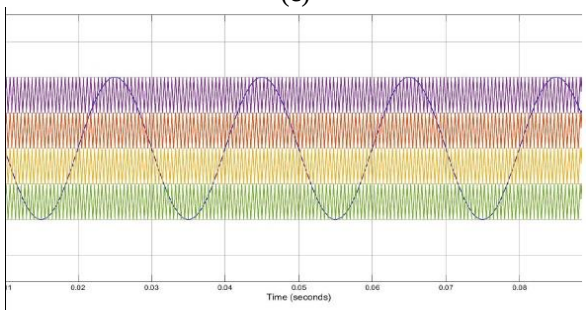
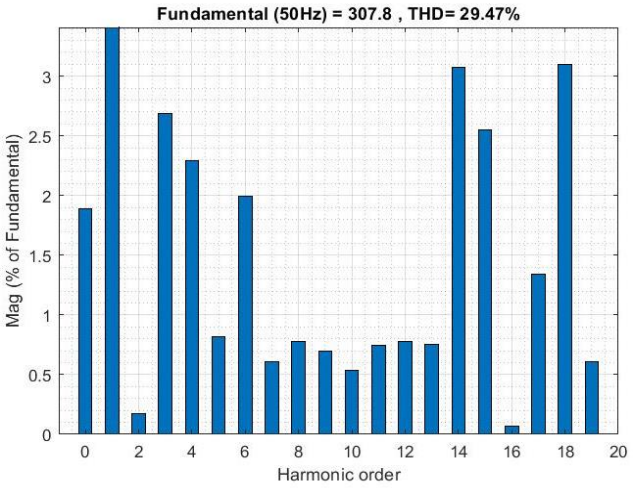



(c)




(d)




(e)

Fig. 11: Continued.

The THD of the three topologies has been determined using different value of modulation index Ma as shown in Fig. 12. The results show that the lowest value of THD can be obtained is 29.47% when the modulation index equal to 1 and can be lowered to 25.74% when the modulation index equal to 1.1.

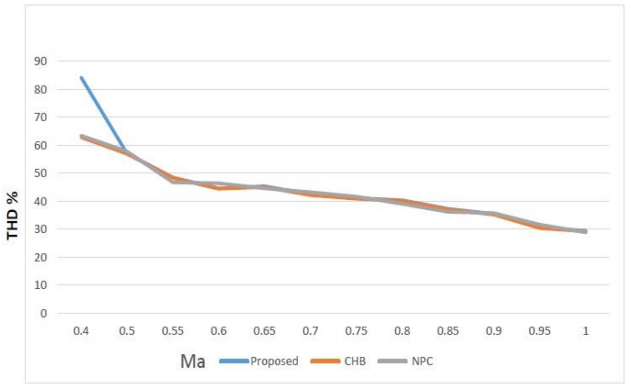



Fig.12: THD vs Ma for Proposed, CHB and NPC five levels inverter

In terms of efficiency, the cascade H bridge inverter efficiency is 83.03%, while it's 79.82% for the neutral clamped inverter. The proposed topology of the five level inverter reaches 98.09% which is the highest as compared to the two conventional topologies.

The comparison analysis for the two conventional MLI topologies has been made under the three different techniques of level shift pulse width modulation and different modulation index values. The results of cascade H-bridge and neutral point clamped MLI are listed and summarized in TABLE II and TABLE III, respectively.

TABLE II

SIMULATION RESULTS OF CHB FIVE LEVEL INVERTER UNDER DIFFERENT MA

| M INDEX | PD | | | | POD | | | | APOD | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | THD% | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% |
| 1 | 29.23 | 307.5 | 7089 | 83.03 | 30.67 | 301.2 | 7085 | 81.76 | 30.69 | 302 | 7105 | 81.67 |
| 0.95 | 30.38 | 296.2 | 6777 | 79.39 | 32.71 | 289 | 6687 | 79.15 | 31.57 | 290.7 | 6733 | 78.96 |
| 0.9 | 35.26 | 277.5 | 6355 | 74.86 | 33.68 | 283.6 | 6395 | 75.22 | 33.28 | 283.9 | 6398 | 75.21 |
| 0.85 | 37.05 | 265.7 | 6000 | 72.66 | 35.65 | 267.7 | 6104 | 72.11 | 36 | 266.6 | 5986 | 72.54 |
| 0.8 | 40.11 | 244.8 | 5617 | 67.99 | 236.5 | 40.76 | 5689 | 67.68 | 236.5 | 40.78 | 5603 | 67.95 |
| 0.75 | 40.9 | 234.6 | 5292 | 65.8 | 227.4 | 43.07 | 5322 | 65.85 | 228.6 | 41.61 | 5307 | 65.9 |
| 0.7 | 42.22 | 215.1 | 4711 | 60.46 | 218.9 | 42.23 | 4681 | 60.37 | 221.8 | 40.86 | 4697 | 60.33 |
| 0.65 | 45.09 | 201.1 | 4432 | 58.57 | 203 | 45.21 | 4459 | 58.74 | 204.6 | 44.37 | 4447 | 58.77 |
| 0.6 | 44.47 | 184.4 | 3915 | 53.21 | 169.5 | 43.1 | 3885 | 53.01 | 172 | 41.8 | 3901 | 53 |
| 0.55 | 48.33 | 173 | 3603 | 52.51 | 163.1 | 45.54 | 3638 | 52.25 | 164 | 46.14 | 3589 | 52.28 |
| 0.5 | 57 | 150.7 | 2982 | 50.09 | 141.6 | 63.82 | 2969 | 50.09 | 150.7 | 57 | 2982 | 50.09 |
| 0.45 | 62.89 | 142.2 | 2671 | 49.78 | 137.7 | 66.09 | 2676 | 49.78 | 142.2 | 62.89 | 2671 | 49.78 |

TABLE II

SIMULATION RESULTS OF NC FIVE LEVEL INVERTER UNDER DIFFERENT MA

| M INDEX | PD | | | | POD | | | | APOD | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | THD% | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% |
| 1 | 29.01 | 306.6 | 7244 | 79.82 | 28.89 | 307.2 | 7244 | 80.12 | 28.38 | 307.6 | 7244 | 80.29 |
| 0.95 | 30.6 | 295.6 | 6875 | 78.4 | 31.65 | 293 | 6876 | 77.13 | 30.55 | 293.9 | 6876 | 77.46 |
| 0.9 | 34.79 | 276.6 | 6580 | 72.28 | 35.76 | 277.9 | 6580 | 73.11 | 35.07 | 278.1 | 6580 | 73.12 |
| 0.85 | 36.68 | 264.2 | 6288 | 69.3 | 36.18 | 265.6 | 6287 | 69.96 | 36.57 | 263.7 | 6287 | 69.03 |
| 0.8 | 39.83 | 246.2 | 5873 | 64.9 | 39.09 | 247.3 | 5873 | 65.42 | 39.25 | 245.9 | 5872 | 64.71 |
| 0.75 | 40.52 | 235.1 | 5554 | 62.56 | 41.68 | 235.6 | 5554 | 62.97 | 40.63 | 235.6 | 5555 | 62.82 |
| 0.7 | 42.97 | 212.2 | 4910 | 57.83 | 43.21 | 211.3 | 4910 | 57.36 | 42.77 | 211.6 | 4910 | 57.55 |
| 0.65 | 44.16 | 202.4 | 4720 | 54.85 | 44.6 | 203.3 | 4720 | 55.38 | 44.34 | 203 | 4720 | 55.22 |
| 0.6 | 46.38 | 181 | 4174 | 49.75 | 46.4 | 179.9 | 4175 | 49.13 | 45.7 | 180.4 | 4174 | 49.38 |
| 0.55 | 48.68 | 172 | 3941 | 47.94 | 46.78 | 172.9 | 3942 | 48.16 | 48.23 | 171.3 | 3941 | 47.55 |
| 0.5 | 58.08 | 150.8 | 3420 | 43.88 | 57.84 | 150.5 | 3421 | 43.7 | 58.08 | 150.8 | 3420 | 43.88 |
| 0.45 | 63.04 | 141.1 | 3143 | 42.48 | 63.46 | 141.1 | 3144 | 42.56 | 63.04 | 141.1 | 3143 | 42.48 |

The cascade H-bridge inverter-based LS-PD has a minimal percentage of THD of 29.23 % and the highest efficiency of 83.03%. While the highest DC power was reached using LS-APOD PWM at 7105 w. The RMS voltage is almost the same using different level shift PWM techniques under different modulation index values as shown in TABLE II.

Neutral point clamped inverter results in TABLE III show that the inverter-based LS-APOD has a minimal percentage of THD of 28.38 % and the highest efficiency obtained of 80.29%. While the highest RMS voltage reached using LS-APOD PWM. The DC power is almost the same using different level shift PWM techniques under different modulation index values.

TABLE IV lists and summarizes the comparison analysis for the proposed five level inverter topology under the three different techniques of level shift pulse width modulation and different modulation index values. The suggested five-level inverter-based LS-APOD has a minimal percentage of THD of 28.9 % and highest DC power of 5976 w. While the highest efficiency reached using LS-PD PWM. The RMS voltage is almost the same using different level shift PWM techniques under different modulation index values.

TABLE IV
SIMULATION RESULTS OF PROPOSED FIVE LEVEL MLI UNDER DIFFERENT MA

| M INDEX | PD | | | | POD | | | | APOD | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | THD% | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% | THD % | VRMS | DC POWER | EFF% |
| 1 | 29.47 | 307.8 | 5924 | 98.09 | 28.95 | 308 | 5966 | 97.76 | 28.9 | 308.4 | 5976 | 97.79 |
| 0.95 | 30.61 | 296.5 | 5533 | 97.95 | 31.69 | 293.8 | 5467 | 97.53 | 31.06 | 294.7 | 5487 | 97.6 |
| 0.9 | 35.51 | 278 | 4910 | 97.5 | 35.81 | 278.8 | 4985 | 97.15 | 35.56 | 279.1 | 4983 | 97.2 |
| 0.85 | 37.31 | 266.1 | 4509 | 97.31 | 36.23 | 266.6 | 4562 | 97.11 | 37.07 | 264.7 | 4503 | 97.05 |
| 0.8 | 40.39 | 245 | 3961 | 97 | 39.19 | 284.4 | 3999 | 96.85 | 39.79 | 247 | 3957 | 96.81 |
| 0.75 | 41.17 | 234.8 | 3619 | 96.87 | 41.7 | 236.7 | 3655 | 96.54 | 41.18 | 236.7 | 3643 | 96.63 |
| 0.7 | 42.51 | 215.5 | 2972 | 96.52 | 43.21 | 212.4 | 2953 | 96.34 | 43.42 | 212.7 | 2961 | 96.38 |
| 0.65 | 45.37 | 201.4 | 2716 | 96.33 | 44.59 | 204.4 | 2747 | 96.16 | 45 | 204.1 | 2739 | 96.16 |
| 0.6 | 44.61 | 184.4 | 2189 | 96 | 46.35 | 181 | 2166 | 95.84 | 45.5 | 181.5 | 2175 | 95.91 |
| 0.55 | 48.52 | 173.1 | 1999 | 95.71 | 46.71 | 174 | 2006 | 95.81 | 49.04 | 172.5 | 1984 | 95.62 |
| 0.5 | 57.09 | 151 | 1609 | 94.58 | 57.65 | 151.7 | 1603 | 94.55 | 58.88 | 151.9 | 1611 | 94.5 |
| 0.45 | 62.7 | 142.3 | 1444 | 93.84 | 63.2 | 142.3 | 1448 | 93.76 | 63.78 | 142.3 | 1445 | 93.76 |

As a result, the proposed five level topology employs fewer switches (6 switches) and one DC voltage supply as compared with the two conventional types of MLI which required (8 switches) for each topology. The switching driving circuit complexity is decreased, the cost is lowered, and the system size is reduced.

## VI. CONCLUSION

This paper presents an analysis for three multilevel inverter topologies. The proposed multilevel inverter topology has been introduced using two of the MLI topologies. CHB and NPC topologies have been used to develop the proposed topology. The proposed system analysis and results have been compared with the other traditional MLI topologies. The results show a satisfied results in terms of THD and efficiency and RMS voltage under different modulation techniques and modulation index values. Another benefits over the two traditional types is reducing the number of switches required to generate five level voltage in MLI and hence reduce the complexity and cost of the designed inverter.

## CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

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