

Nonconventional Diode Clamped Multilevel Inverter with Reduced Number of Switches

Adala O. AbdAli *, Ali K. Abdulabbas, Habeeb J. Nekad
Electrical Engineering Department, University of Basrah, Basrah, Iraq

Correspondence

*Adala Ouda Abdali
Electrical Engineering Department,
University of Basrah, Basrah, Iraq.
Email: eng.adala@gmail.com

Abstract

The conventional multilevel inverter (MLI) is divided into three types: diode clamped MLI, cascade H Bridge MLI and flying capacitor MLI. The main disadvantage of these types is the higher required number of components when the number of the levels increases and this results in more switching losses, system higher cost, more complex of control circuit as well as less accuracy. The work in this paper proposes two topologies of nonconventional diode clamping MLI three phase nine levels and eleven levels. The first proposed topology has ten switches and six diodes per phase while the second topology has nine switches and four diodes per phase. The pulse width modulation (PWM) control method is used as a control to gate switches. THD of the two proposed topologies are analyzed and calculated according different values of Modulation index (where the power loss and efficiency are obtained and plotted).

KEYWORDS: multilevel inverter, nonconventional Diode Clamped inverters, HPWM.

I. INTRODUCTION

A multilevel inverter is power electronic configuration that has received much attention from researchers because it became one of the most widely used in the electric field [1,2]. Multilevel inverter generates output voltage that is staircase waveforms “start from three levels that can increase number of levels by increasing number of devices and feeding more dc source [3]. The need to use multilevel inverter is appeared because the output voltage and power increases while harmonic content decreases [4,5].

Multilevel inverter can be divided to two different categories depending on the circuit configuration: Conventional and Nonconventional types. Each category has three well known types of multilevel inverter named as diode clamped multilevel inverter, cascade H bridge multilevel inverter and flying capacitor multilevel inverter [6-9].

The disadvantage of conventional multilevel inverter is that its need for more number of components such as switches, clamping diodes and capacitors and this leads to increase the number of levels which causes higher cost and more complexity drive circuit [10-15]. Nowadays multilevel inverter is used widely in high power industry medium-high voltage applications in recent times. So that a lot of configuration and topologies are proposed to fix this problem such as the proposed solution in [16] to obtain nine levels by using 12 clamping diodes and 12 switches in the modified structure instead of 14 clamping diodes and 16 switches in conventional diode clamped where the number of clamping diodes $2(m-2)$ for m levels circuit voltage.

Zhiguo in his research [17], proposed a novel topology that combines two levels and three levels by using two diodes. This topology reduced the excessive number of clamping diode and make the system more expensive but extendable to a multilevel inverter as well as easy to control for a higher number of levels.

In this paper, two proposed topologies for diode clamped with reduce number of device and two pulse width modulation (PWM) control are presented to gate switches and to produce 9 levels output voltage in the first topology and 11 levels in the second topology. While the two topologies can be easily extended to multilevel inverter with higher number of levels, finding THD, modulation index (Ma) for every type then comparison with the conventional diode clamped

II. CONVENTIONAL DIODE CLAMPED

One of the common multilevel configurations is diode clamped which has low voltage switching devices that are arranged in a series to produce high output voltage levels and high efficiency. An m -level consist of $(m-1)$ number of DC link capacitors, $2(m-1)$ number of switching devices, and $2(m-2)$ number of clamping diodes. The number of levels can be increased to higher levels by increasing the number of devices which results in the output voltage closer to sinusoidal waveform. Although the output voltage is improved but this considered as a disadvantage because the excessive number of clamping diodes leads a higher system cost and more complexity in the system control [18,19].



This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

© 2020 The Authors. Published by Iraqi Journal for Electrical and Electronic Engineering by College of Engineering, University of Basrah.

III. NONCONVENTIONAL DIODE CLAMPED NINE LEVELS PROPOSED TOPOLOGY

The proposed topology contains a minimum number of switches for generating the same output levels as compared with conventional multilevel inverter [20] as shown in Fig. (1) :

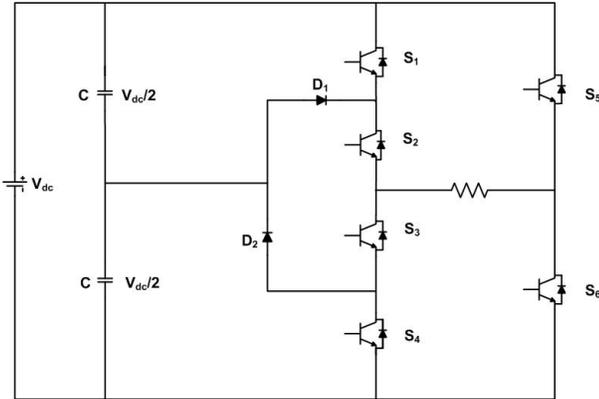


Fig. (1) Basic Circuit of one phase diode clamped 5- Level.

The proposed diode clamped can produce 5-level output with only a single DC source, two diodes, six switches and two capacitors which is less in the numbers of elements when comparing with conventional diode clamped for same levels. Figure(1) shows one phase of circuit. The load is connected between midpoints (S_2 & S_3) and (S_5 & S_6), where S_6 is turned always ON during positive half cycle of output voltage where as S_5 is turned ON during the negative half cycle. Switches S_5 and S_6 are used to complete the cycle of the current because these are connected to the DC source. In order to produce higher output voltage levels (m), the number of switches (N_s), number of capacitors (N_c) and number of diodes (N_D) are extended according to the following equations :

$$N_s = (m + 1) \tag{1}$$

$$N_c = \left(\frac{m - 1}{2}\right) \tag{2}$$

$$N_D = (m - 3) \tag{3}$$

In this paper, nine level output voltage can present as shown in Fig.(2) and many modulation techniques are used for producing switching pulses in this proposed inverter that uses multilevel PWM technique.

This technique compares between four high frequency triangular carrier with rectified sinewave to produce the switching pulses to generate 9 level as shown in Fig.(4).

For analytic purposes, one phase of diode clamping to get 9 levels output voltage can be divide into four modes of operation depending on the time interval as shown in Fig.(4):

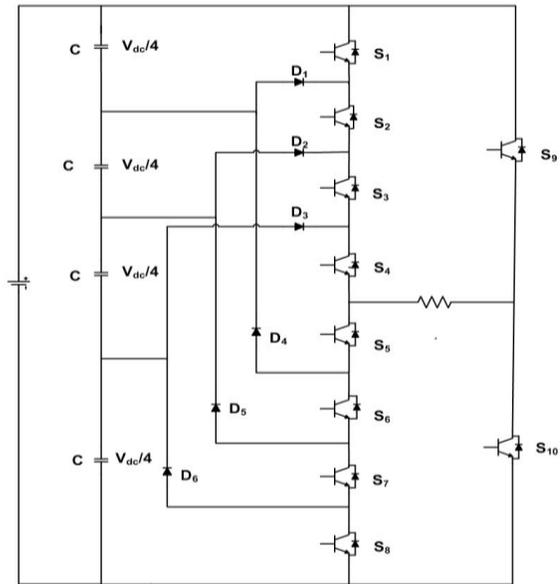


Fig. (2) Extended Circuit of 9-levels diode clamped inverter

Mode (1) time interval $0 < t < t_1$ & $t_6 < t < t_7$

In this mode, switches (S_4 and S_{10}) are triggered ON with all other switches are left OFF so that one capacitor will be associated with the load and therefore one quarter of the input supply has on the load ($V_{out} = \frac{V_{dc}}{4}$) as shown in Fig (3-a)below.

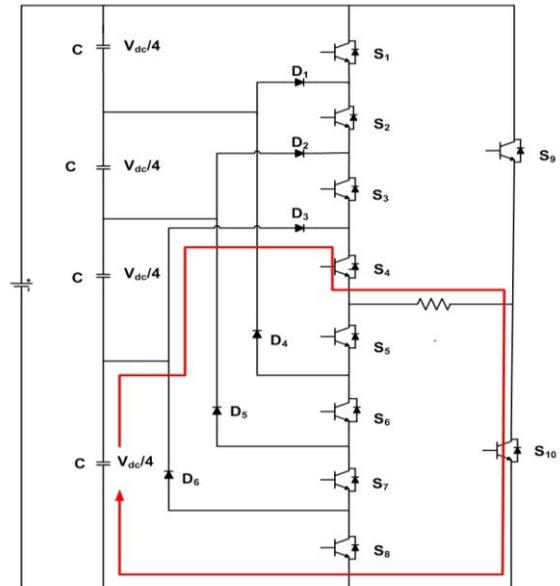


Fig. (3-a): Mode (1) Operation of Circuit

Mode (2) time interval $t_1 < t < t_2$ & $t_5 < t < t_6$

Switch S_3 will be turned ON while other switches are in the previews mode so two capacitors are connected to load then output voltage is a half of the input source value ($V_{out} = \frac{V_{dc}}{2}$) as shown in Fig.(3-b)

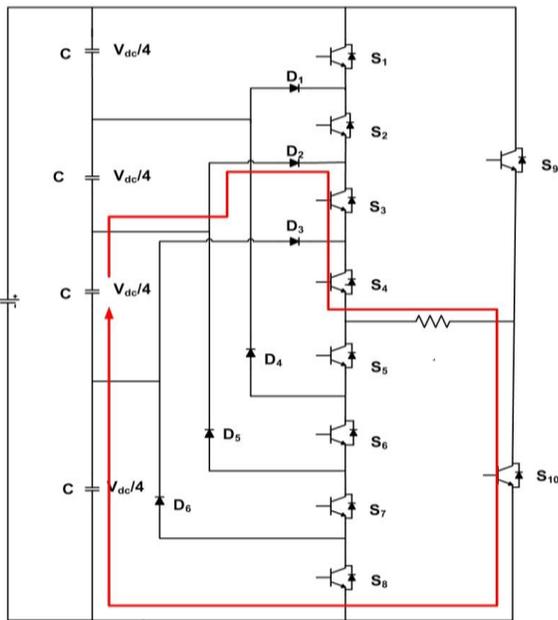


Fig. (3-b): Mode (2) operation of circuit

Mode (3) time interval $t_2 < t < t_3$ & $t_4 < t < t_5$
 In this mode switch S_2 is triggered ON with the rest of the switches in previous state so that the load is connected to three capacitors and therefore the output voltage is equal to three quarters of the input source voltage ($V_{out} = \frac{3V_{dc}}{4}$) as shown in Fig.(3-c)

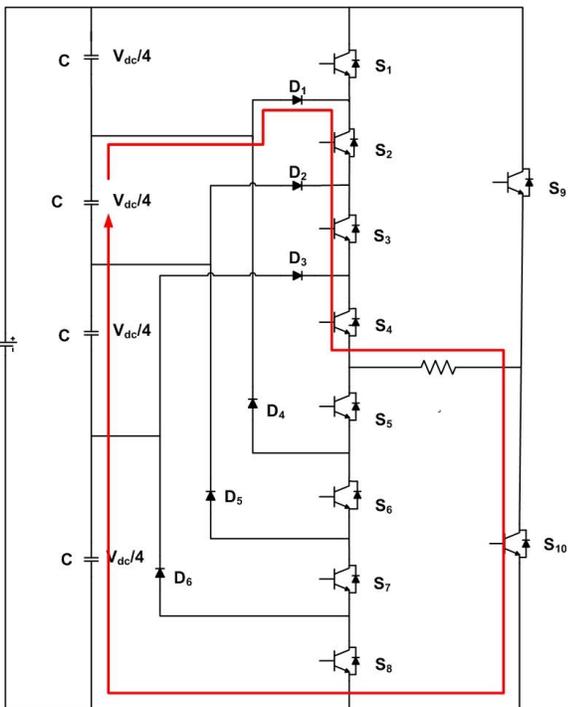


Fig. (3-c): Mode (3) operation of circuit

Mode (4) time interval $t_3 < t < t_4$
 All switches on the top of the circuit are on the ON state so that the output voltage equal to the source input voltage When ($V_{out} = V_{dc}$) as shown in Fig.(3-d)

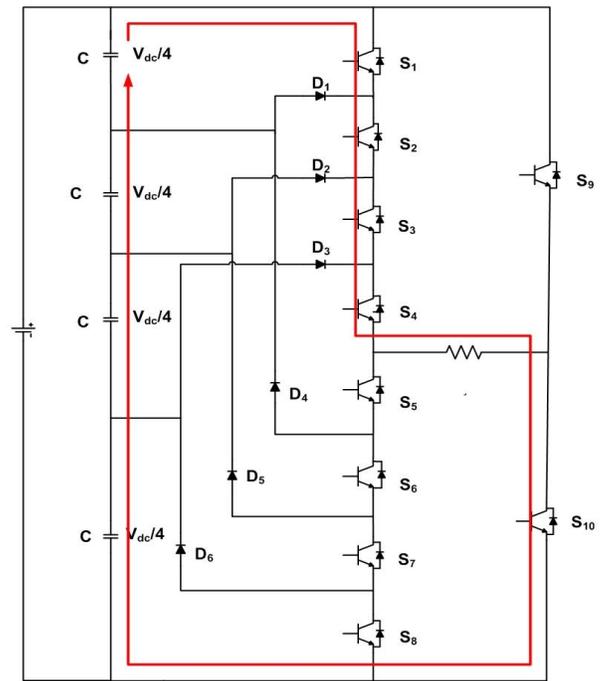


Fig. (3-d): Mode (4) operation of circuit

The same way to get negative half cycle in compared reference wave with the four triangular carrier but start in the reverse period.

IV. SIMULINK AND CONTROLLING NONCONVENTIONAL 9-LEVEL DIODE CLAMPED

Nonconventional diode clamped is connected to three phases where each phase is contained ten switches, six diodes and four capacitors, Fig (2) represents one phase connection. Three phases is connected to the load and all these are feeding by one DC source. To control the switching signal, PWM technique is used by comparing the absolute sine wave(reference) with four triangular waves(carrier) as shown in Fig (4)

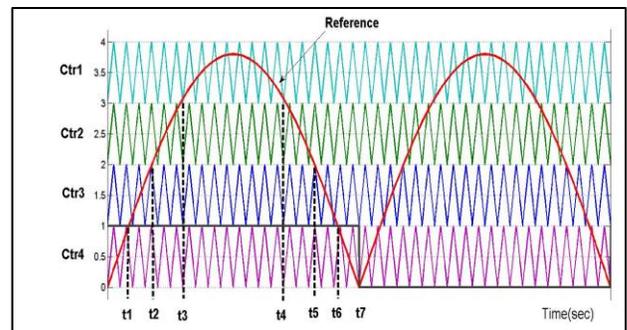


Fig. (4): PWM control method used for 9-level diode clamped

The pulse generator has pulse width 50% of period with amplitude 1V and period 0.02 sec. The output of the pulse generator feeder S_{10} and the complement feeder is S_9 . Fig.(5) represents the Simulink of firing pulse generation of switching. The absolute sinewave is compared with four

carrier (triangular wave high frequency) to trigger the switching process.

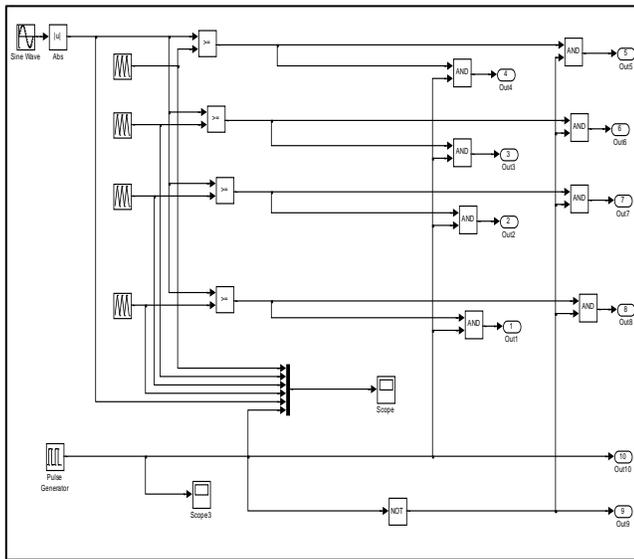


Fig. (5): Firing pulse generation of switching

The output voltages for phase (a, b and c) are ac voltage which is staircase and consist nine levels with phase shift of -120 and 120 for phase b and c respectively as shown in Fig (6).

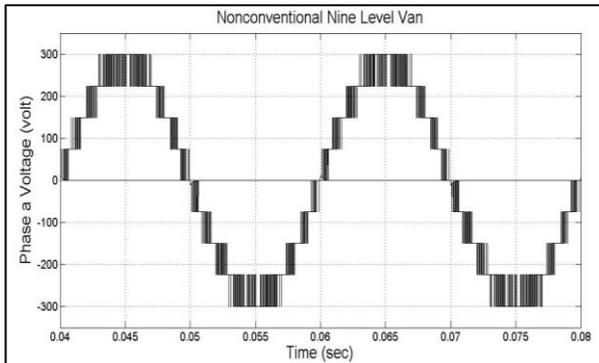


Fig. (6-a)

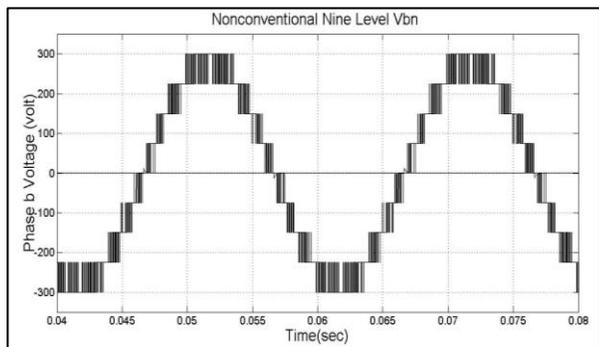


Fig. (6-b)

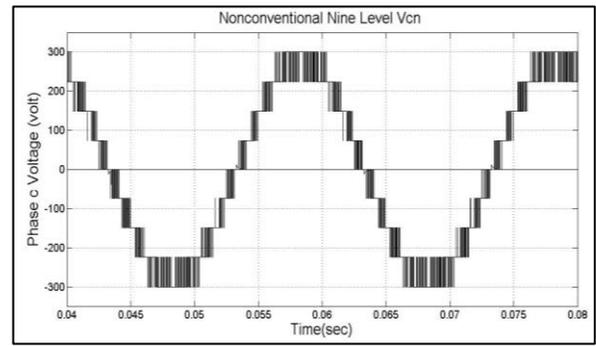


Fig. (6-c)

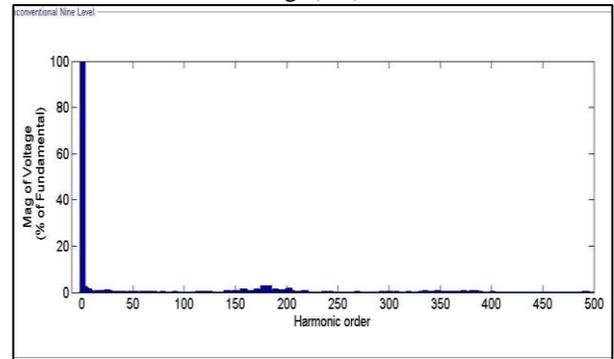


Fig. (6-d)

Fig. (6): Simulations result a) Output Voltage phase a. (b) output voltage phase b (c) output voltage phase c (d) THD for one period of phase a

The least value of THD at nonconventional nine levels is 11.5% at M_a equals to 0.55. Notice that the fundamental harmonic is only appear and other harmonics are eliminated. It is also worth noting that when two the circuits of conventional and nonconventional are operating at high value of switching frequency, in particular 18000 Hz, the least value of THD is 11.5% at modulation index (M_a) is 0.55 as shown in Fig (7). At this value of M_a , Fig (8) shows the values of THD with variable values of switching frequency and compared with conventional nine levels NPC

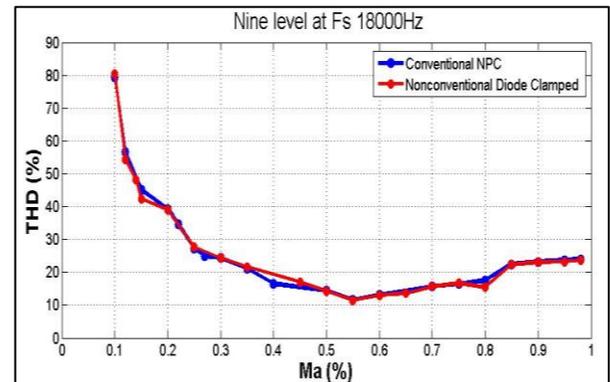


Fig. (7) : Change THD with M_a for Constant Switching Frequency

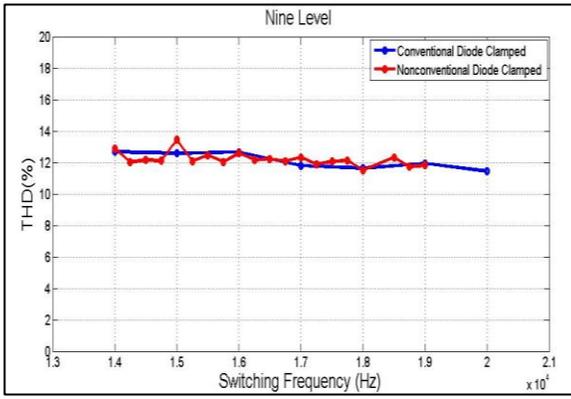


Fig. (8): Change THD With Switching Frequency at Ma equal 0.55

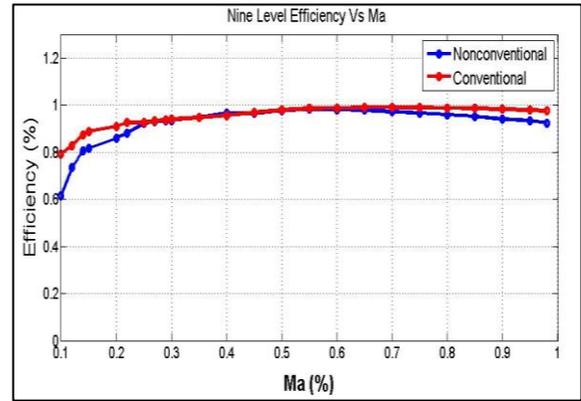


Fig. (11): Change Efficiency With Ma at Constant Switching Frequency

RMS voltage increases linearly at small value of Ma while remains constant at large values of Ma as shown in Fig (9)

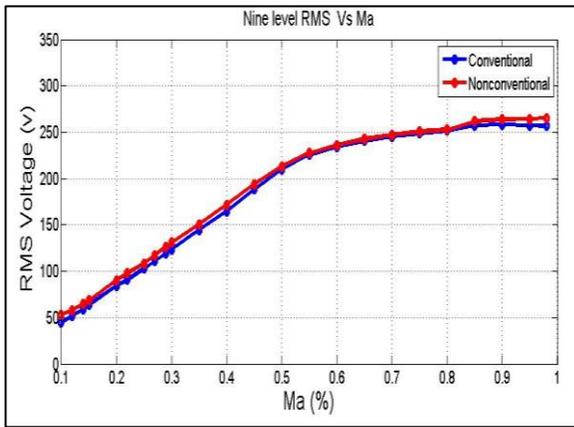


Fig. (9): Change RMS with Ma at Constant Switching Frequency

Multilevel inverters are used to produce high voltage and high power ability with less harmonic, but requires more number of devices which leads to increase of switching loss and decreases the efficiency, so that in Fig(10) the power loss in conventional is high than nonconventional but the efficiency is convergent because the input power for conventional one is larger than nonconventional as shown in Fig.(11).

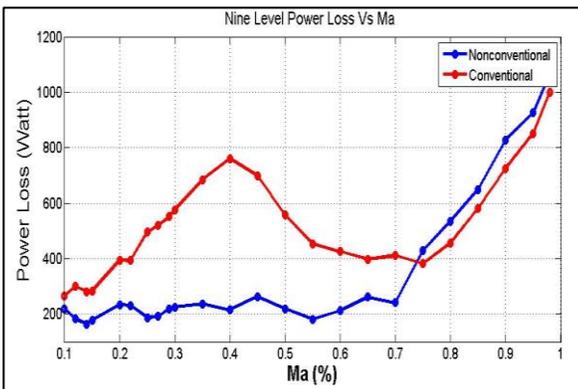


Fig. (10): Change Power Losses with Ma at Constant Switching Frequency

V. HYBRID NPC MULTILEVEL INVERTER

Same performance algorithmic between space vector PWM theory and triangle comparison PWM, so that it named Hybrid PWM(HPWM), the block diagram of HPWM illustration in Fig. (12)[21]

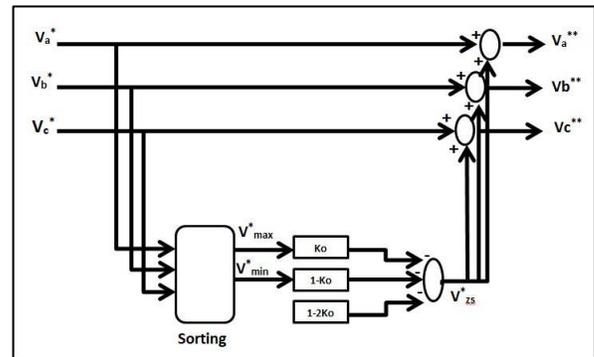


Fig. (12): Block diagram HPWM

The Simulink block diagram is represented in Fig (13) where Va^*, Vb^*, Vc^* denote to the sinusoidal voltages for phase a, b and c that have phase shift 0, -120 and 120 respectively. For every time interval, it can be considered these voltages values (Va^*, Vb^*, Vc^*) max, mid and min values. To apply the zero sequence equation: $Vzs^* = [(1 - 2K_0) + K_0Va^* + (1 - 2K_0)Vc^*]$ where Va^* is max value and Vc^* min value then sum (Va^*, Vb^*, Vc^*) with Vzs^* are given ($Va^{**}, Vb^{**}, Vc^{**}$)

where $Va^{**}, Vb^{**}, Vc^{**}$ input reference voltage is compared with carrier signals to gate switches as shown in Fig.(14).

Va^{**} describe by equation:

$$Va^{**} = Va^* + [(1 - 2K_0) + K_0Va^* + (1 - 2K_0)Vc^*] \quad (4)$$

$$Va^{**} = va^* + Vzs^* \quad (5)$$

Where $0 \leq k_0 \leq 1$ is a factor can be constant or variable and effect the voltage wave,

Va^{**} and Vc^{**} is represent V_{max}^* and V_{min}^* respectively as shown in Fig(12)

Vzs^* is zero sequence component

$$Vzs^* = [(1 - 2k_0) + k_0Va^* + (1 - 2k_0)Vc^*] \quad (6)$$

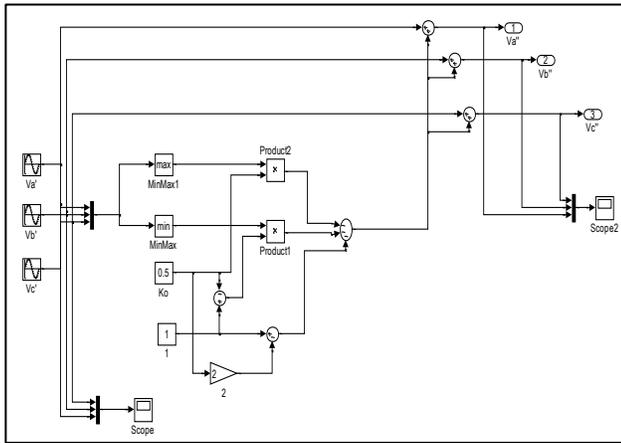


Fig. (13): Simulink HPWM configuration For Reference Voltage

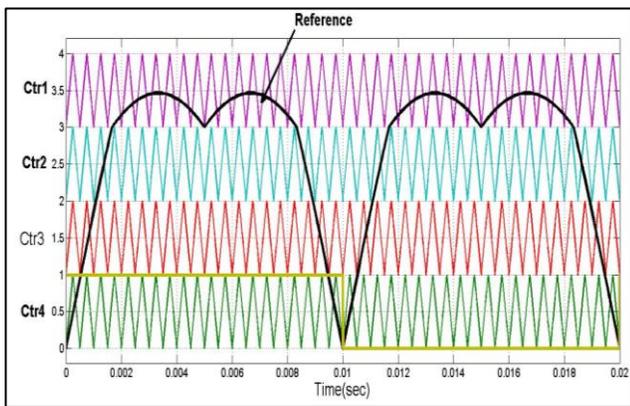


Fig. (14): PWM control method 9 level used HPWM

From equation, it is noticed the zero-sequence component is added to the three-phase sinusoidal modulating signal which leads the inverter fundamental voltage increment without causing over modulation.

Note that when the three phase HPWM nine levels diode clamped is operated at switching frequency (F_s) equals to 19500 Hz and at modulation index (Ma) is 0.6, it is recorded that the least value of THD is 20.66% as shown in Fig.(15). Comparing with conventional HPWM nine levels diodeclamped at the same switching Frequency the least value of THD is 20.7% at $Ma=0.6$.

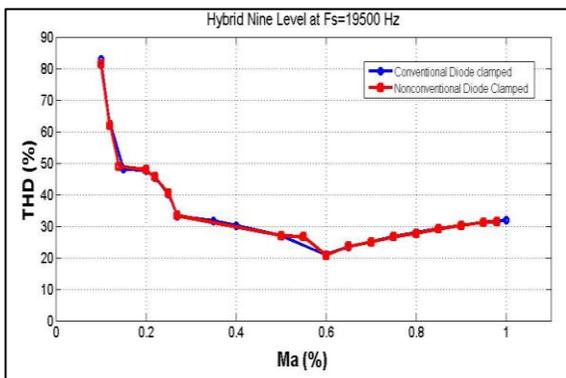


Fig. (15): Change THD with Ma at Constant Switching Frequency

At the same value of $Ma=0.6$, the circuit of Hybrid nonconventional three phase nine levels is running with many values of switching frequency exhibits equivalent performance with the conventional three phase at the same value of levels, However, the conventional circuit have a large number of switches and diode clamped elements in comparison with the nonconventional circuit as shown in Fig (16) .

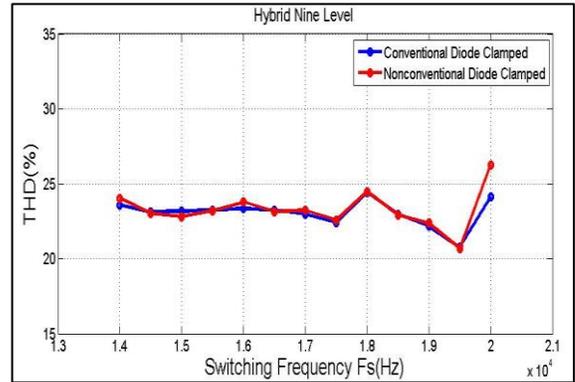


Fig. (16): Change THD With Switching Frequency at Ma equal 0.6

Because of the large number of devices for conventional circuit which are reflected on the results as shown in Fig (17) the power loss is larger than non conventional and it is increased with the increased amplitude of the absolute sinwave .

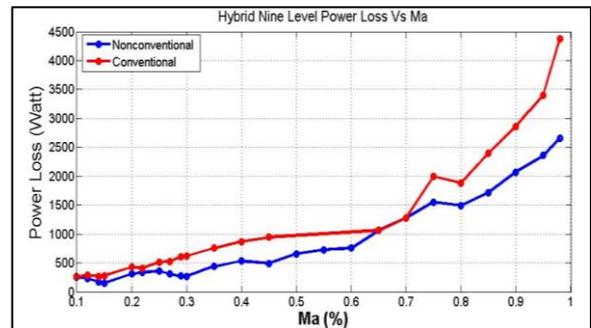


Fig. (17): Change Power Loss With Ma at Constant Switching Frequency

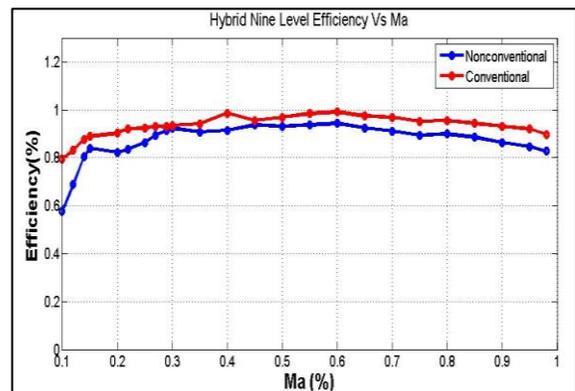


Fig. (18): Change Efficiency with Ma at Constant Switching Frequency

From Fig(18) the efficiency of the conventional model is a little higher than the nonconventional one when the input power is larger than nonconventional . RMS output voltage value is raised with the increase of Ma for the two HPWM circuits conventional and nonconventional as shown in Fig (19)

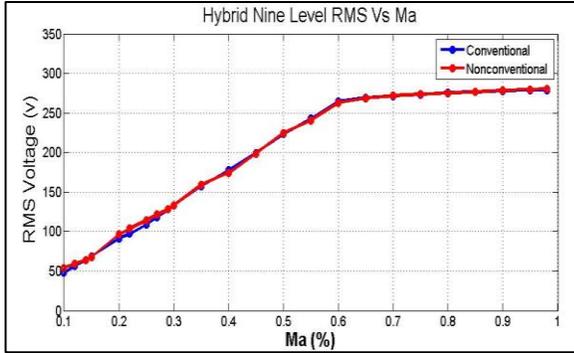


Fig. (19): Change RMS Voltage with Ma at Constant Switching Frequency

VI. NONCONVENTIONAL DIODE CLAMPED ELEVEN LEVELS PROPOSED TOPOLOGY

Eleven level topology of one phase inverter present in Fig. (20)[22]:

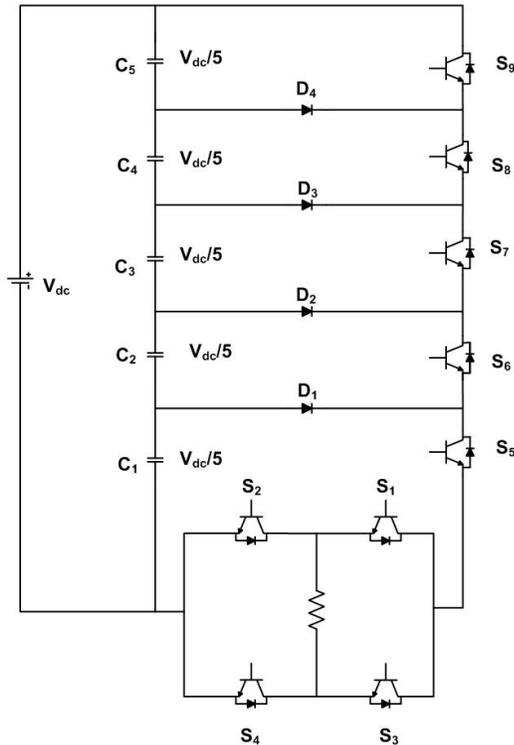


Fig. (20): One Phase structure for 11-Level diode clamped

which are half the number is compared to conventional topology. DC voltage is divided into five dc bus capacitors. The circuit produce eleven levels output voltage. It is contained only one dc voltage source, nine switches, five capacitors and four diodes clamped that can be extended to number of levels according to the following equations:

$$N_c = \frac{m - 1}{2} \tag{7}$$

and Number of switches N_s :

$$N_s = \frac{m+7}{2} \tag{8}$$

and Number of diodes: N_d

$$N_d = \frac{m - 3}{2} \tag{9}$$

Where m is number of levels.

One phase of diode clamping to get 11 levels output voltage can be divide into five modes of operations depending on the time interval shown in Fig (22):

Mode (1) For time interval $0 < t < t_1$ & $t_8 < t < t_9$

In this mode, S_5 is turned ON and (S_1 and S_4) are always turned ON during positive half cycle so C_1 is connected and all other switches are OFF. The voltage at the load is $(V_{out} = \frac{V_{dc}}{5})$ as shown in Fig. (21-a).

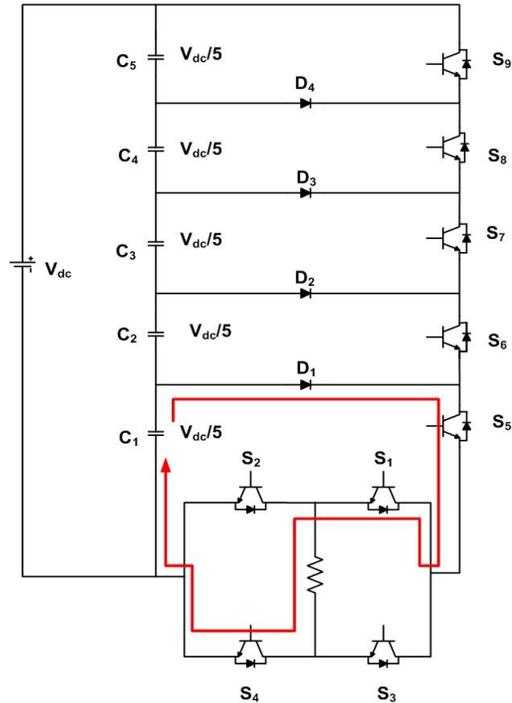


Fig. (21-a): Mode (1) operation of circuit

Mode (2) For time interval $t_1 < t < t_2$ & $t_7 < t < t_8$

During this interval, S_6 and S_5 are turned ON and still (S_1 and S_4) are turned ON and all other switches OFF, C_1 and C_2 are connected to terminal switches (S_4 and S_5) respectively the voltage at the load become $(V_{out} = \frac{2V_{dc}}{5})$ as shown in Fig. (21-b).

Mode (3) For time interval $t_2 < t < t_3$ & $t_6 < t < t_7$

When (S_5, S_6 and S_7) are tuned ON and all other switches are OFF the voltage at the load is $(V_{out} = \frac{3V_{dc}}{5})$ produced from

connecting three capacitors (C_1 , C_2 and C_3) as illustrated in Fig. (21-c)

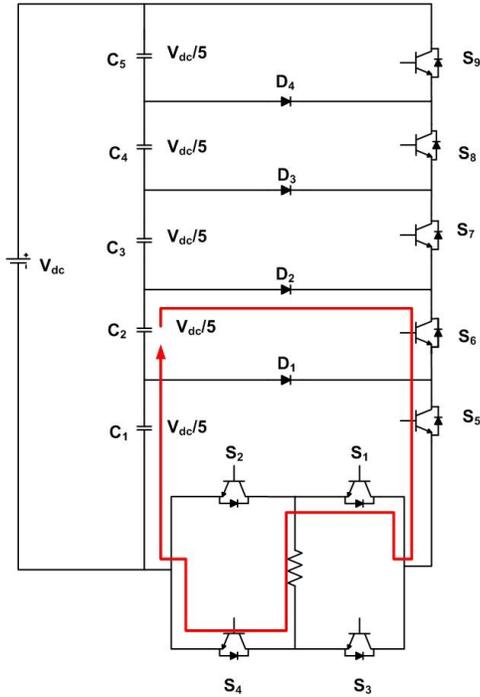


Fig.(21-b): Mode (2) Operation of circuit

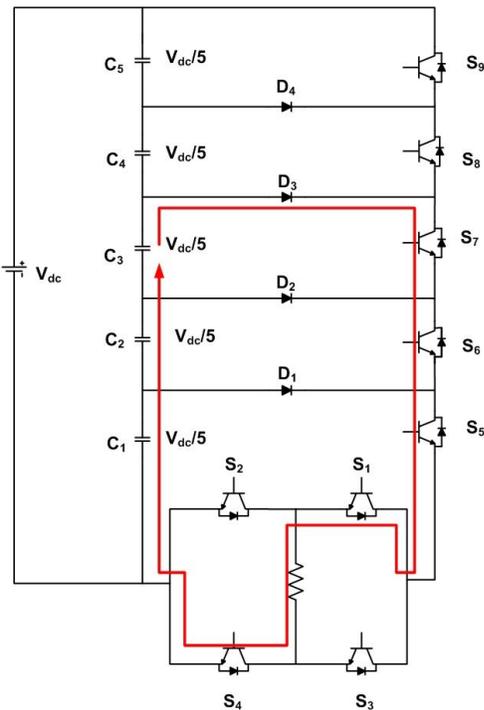


Fig. (21-c): Mode (3) operation of circuit

Mode (4) For time interval $t_3 < t < t_4$ & $t_5 < t < t_6$ When (S_1, S_4, S_5, S_6, S_7 and S_8) are switched ON and all other switches OFF, the capacitors (C_1, C_2, C_3 and C_4) are

connected to the switches which triggered this lead the voltage at the load is $V_{out} = \frac{4V_{dc}}{5}$ as shown in Fig. (21-d).

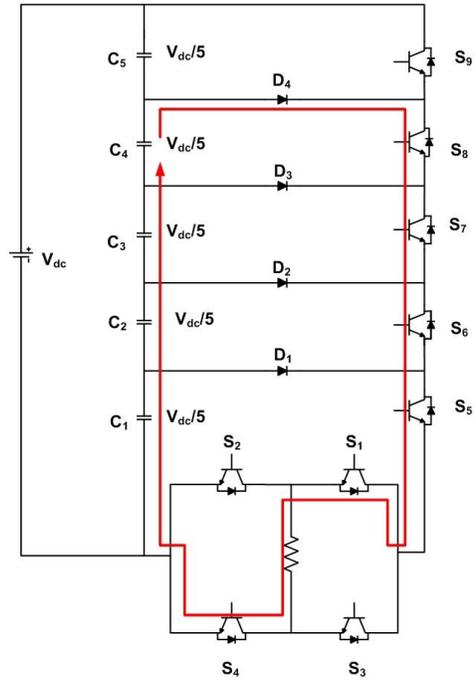


Fig. (21-d): Mode (4) operation of circuit

Mode (5) For time interval $t_4 < t < t_5$ In this interval ($S_1, S_4, S_5, S_6, S_7, S_8$ and S_9) are turned ON while still (S_2, S_3) are OFF the voltage at the load is ($V_{out} = V_{dc}$) from connected as shown in Fig. (21-e).

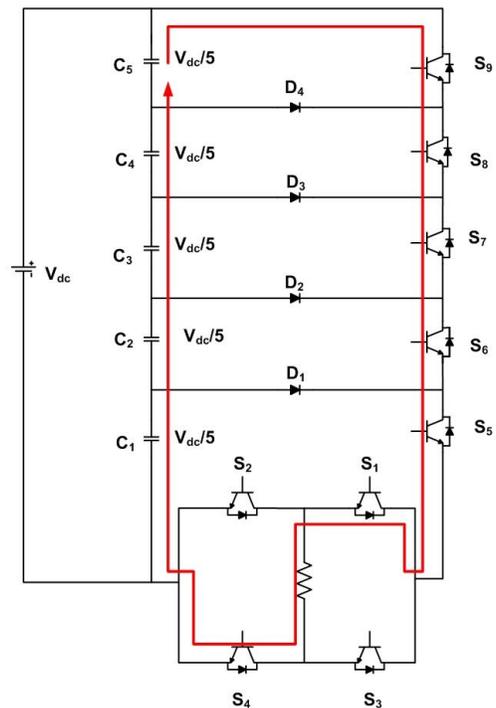


Fig. (21-e): Mode (5) operation of circuit

The same way is repeated for negative half cycle for reverse interval of the time, when the two switches (S_2 and S_3) are gating in the negative cycle.

VII. SIMULINK AND CONTROLLING NONCONVENTIONAL DIODE CLAMPED 11-LEVEL

Three phase 11-level nonconventional diode clamped inverter, and three legs are connected to the load, the circuit is feeding by one DC source, the same PWM technique in previous circuit is used but five carrier signals that is comparator with rectified sinewave to generate pulses which are gating switches (S_5, S_6, S_7, S_8, S_9). The switches (S_1 & S_4) are ON during the positive half cycle while (S_2 & S_3) are gated ON in the negative half cycle, so that in the Simulink is used pulse generation with the pulse width 50% off period for controlling S_1, S_2, S_3 and S_4 as shown in Fig. (23).

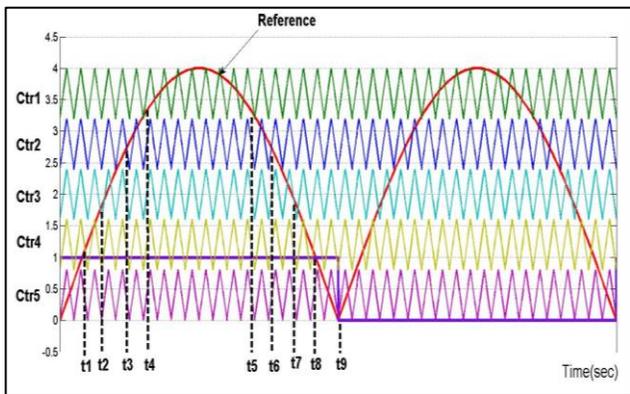


Fig. (22): PWM control method used for 11-level diode clamped inverter

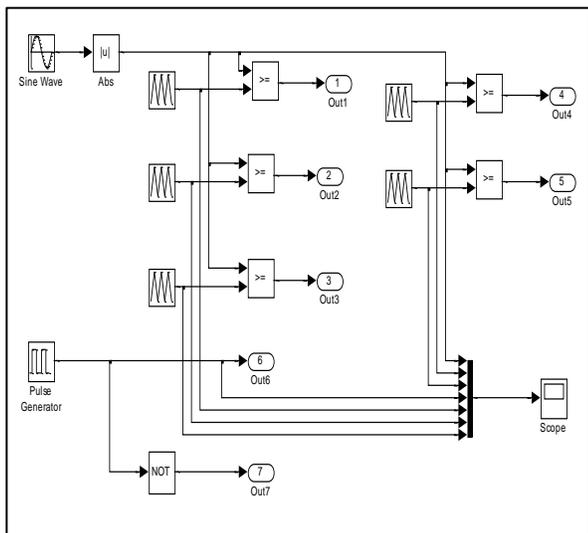


Fig. (23): Firing Pulse generate of switching

The output voltage for phase a, as shown in Fig(24-a), is consisted of eleven levels, phase (b and c) at the same output levels but phase shift -120, 120 respectively illustrate in Fig (24-b) and Fig (24-c)

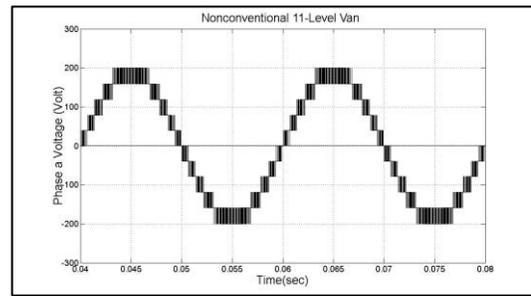


Fig.(24-a)

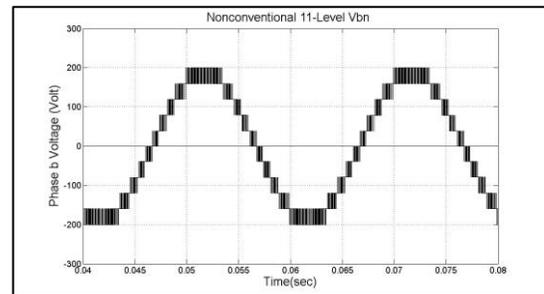


Fig.(24-b)

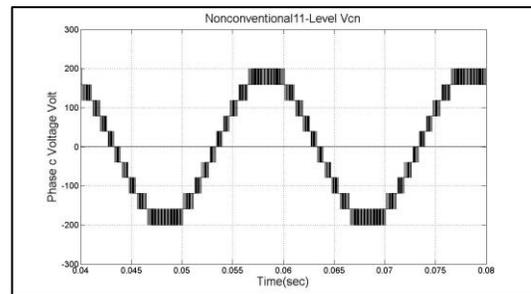


Fig. (24- c)

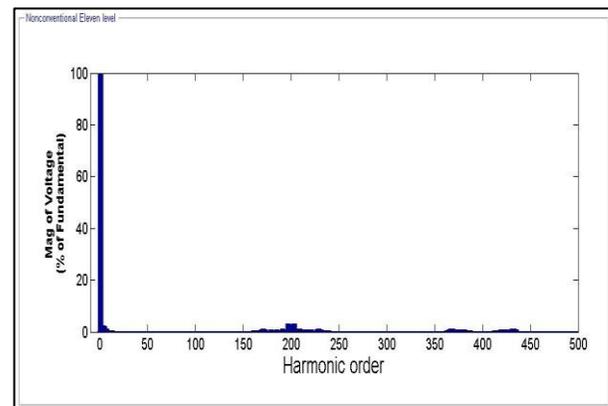


Fig.(23-d)

Fig. (24): Simulations result a) Output Voltage phase a. (b) output voltage phase b (c) output voltage phase c (d) THD for one period of phase a

When this circuit is operating at high values of Frequency equal 20000Hz ,as well known the multilevel inverter is used to improve the output voltage ,the output voltage was produced with minimum THD as shown in Fig (24-d) the fundamental value is high and under control , other harmonics have very small values so that do not need filtering process.

For many values of modulation index, it is clear when modulation index has a value of 0.45, THD is recorded less value which is 9.77 % when the circuit operate at switching frequency 20000 Hz as illustrated in Fig (25)

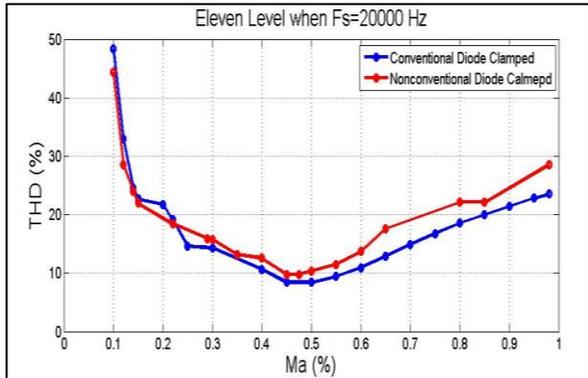


Fig. (25): Change THD with Ma at Constant Switching Frequency

Fig (26) shows the circuit of the three phase eleven levels diode clamped operates at $Ma=0.45$ with variable value of switching frequency and THD is recorded and compared against the conventional circuit under similar circumstances as shown in Fig (26)

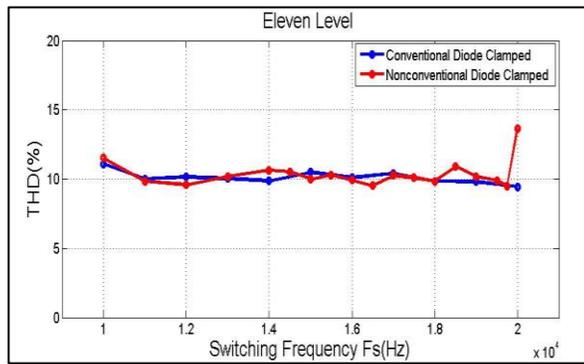


Fig. (26): Change THD with Switching Frequency at Modulation index equal 0.47

The efficiency for conventional and nonconventional for the same levels are converged but the nonconventional circuit need a large number of devices and with more connections as shown in Fig (27)

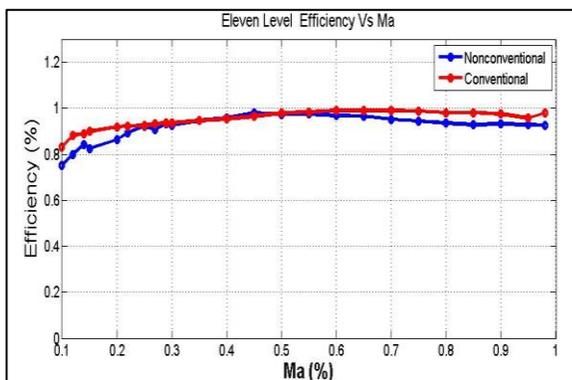


Fig. (27) Efficiency Via Ma Diode Clamped

The same result for hybrid circuit the efficiency is high as shown in Fig(28)

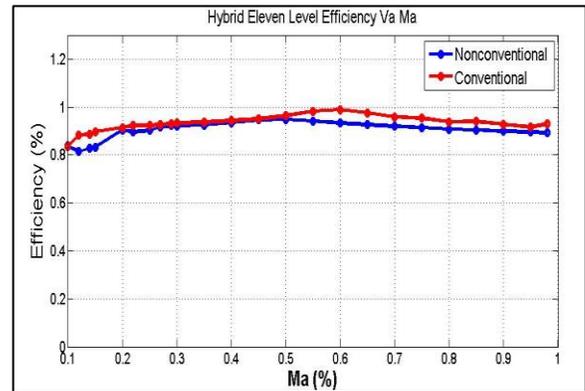


Fig. (28):Change Efficiency with Ma at Constant Switching Frequency

The power loss in the conventional circuit is more than nonconventiona, at the same conditions for HPWM circuit .

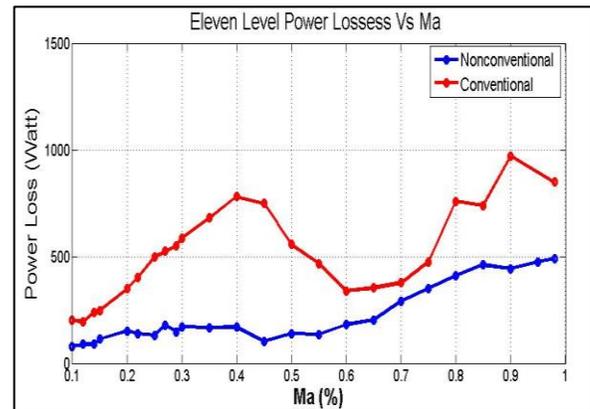


Fig. (29): Change Power Loss with Maat Constant Switching Frequency For Diode Clamped

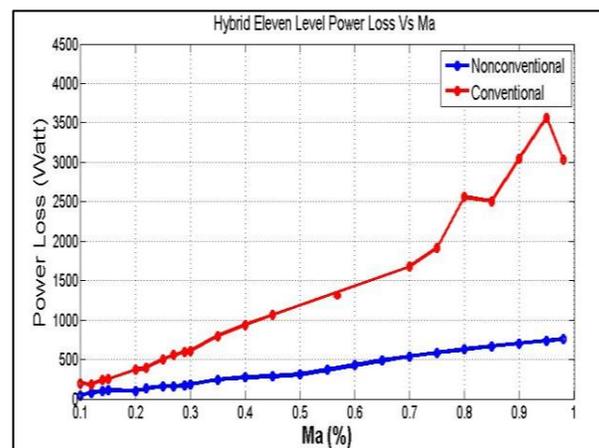


Fig. (30):Change Power Loss with Maat Constant Switching Frequency For HPWM Diode Clamped

A large number of switches and a large number of carriers that use for firing switching in the conventional three phase eleven levels, all this results in increasing the RMS voltage

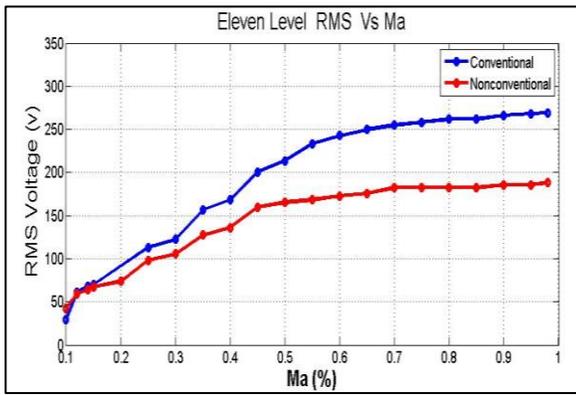


Fig. (31):Change RMS Voltage with Ma at Constant Switching Frequency Diode Clamped

The RMS voltage for eleven levels conventional circuit is large than nonconventional one

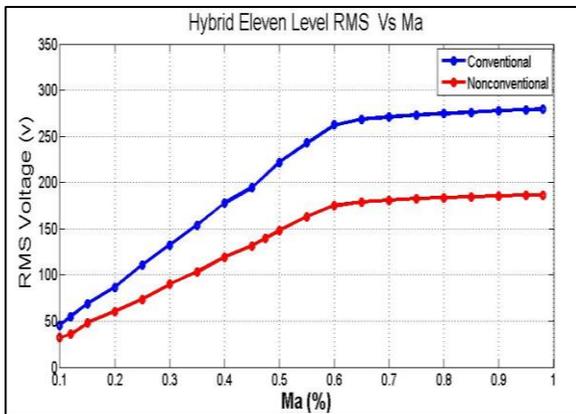


Fig. (32):Change RMS Voltage with Ma at Constant Switching Frequency HPWM Diode Clamped

The main differences between the conventional diode clamped and the two proposed nonconventional topologies, advantage and disadvantage can be illustrated in the Table (I).

VIII. CONCLUSIONS

This paper has presented two circuit that are used to produce m levels of the output voltage with a smaller number of switches and diode clamped in comparison with conventional diode clamped MLI. The proposed circuits can be extended to high number of levels without any higher cost and difficulty with control system. It is clear that the THD is less than conventional diode clamped, and the output voltage is staircase that is closed to the sine wave when number of levels are increased. It is wide in the conventional nine and eleven levels 16 and 20 switches , 14 and 18 Diodes and 8 and 10 capacitors for one phase in the circuit , while in the nonconventional for the same levels has 10 and 9 switches, 6 and 4 Diodes, 5and 4 capacitors ,respectively, for one phase. The size of conventional inverter is bigger because of the large number of devices where the switching loss is increased and the efficiency is decreased. Furthermore, the connections of the circuit are complex to control. The details

in TABLE I clarify the comparison between conventional and nonconventional diode clamped.

TABLE I
COMPARISON BETWEEN CONVENTIONAL AND NONCONVENTIONAL DIODE CLAMPED FOR M LEVELS

Item	Conventional diode clamped	Non-conventional First proposal	Non-conventional Second proposal
No. of switches	$2(m-1)$	$m+1$	$\frac{m + 7}{2}$
No. of clamping Diode	$2(m-2)$	$m-3$	$\frac{m - 3}{2}$
No. Of DC link Capacitor	$m-1$	$\frac{m - 1}{2}$	$\frac{m - 1}{2}$
Voltage of each capacitor	$\frac{V_{dc}}{m - 1}$	$\frac{2V_{dc}}{m - 1}$	$\frac{2V_{dc}}{m - 1}$
Advantage	Produce high voltage and high-power capability	Less number of devices, Less THD, low switch loss and no complex to control	Also, less THD and low switch loss, no complex to control also the switching operate at high frequency the number of devices is less than conventional
Dis-advantage	Increase number of levels cause increase switch loss and cost the system as well as difficult to control	The efficiency is convergent with values of conventional circuit with same levels	The efficiency is convergent with values of conventional circuit with same levels

CONFLICT OF INTEREST

The authors have no conflict of relevant interest to this article.

REFERENCES

- [1] K. Boora and J. Kumar, "A novel cascade asymmetrical multilevel inverter with reduce number of switches," *IEEE transection on industry applications*, vol. 55, no. 6 ,pp.7389-7399, November / December 2019.
- [2] A. Chen and X. He, "Research on hybrid-clamped multilevel-inverter topologies," *IEEE Transactions On Industrial Electronics*, vol. 53, no. 6,pp. 1898-1907, December 2006.
- [3] A. Bendre, G. Venkataramanan, D. Rosene and V. Srinivasan, " Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *IEEE Transactions on industrial electronics*, vol. 53, no. 3,pp. 718-726, June 2006
- [4] N. Susheela, P. Satish Kumar and S.K.Sharma, "Generalized algorithm of reverse mapping based svpwm strategy for diode clamped multilevel inverters," *IEEE Transactions on industrial electronics*, TIA2018
- [5] S. S. Lee, C. S. Lim and K-B. Lee, "Novel active-neutral-point-clamped inverters with improved voltage-boosting capability," *IEEE Transactions on industrial electronics*, TPEL.2019.
- [6] J. Zhao, X. He and R. Zhao, "A novel PWM control method for hybrid-clamped multilevel inverters," *IEEE transactions on industrial electronics*, vol. 57, no. 7, pp.2365-2373, JULY 2010.
- [7] Z. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefanovic, J. M. (Mickey) Leuthen and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Transactions on industry applications*, vol. 41, no. 6, pp.1698-1706, November/December 2005.
- [8] E.Babaei, S. Alilu, and S.Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed h-bridge," *IEEE Transactions on industrial electronics*, vol. 61, no. 8, pp.3932-3939, August 2014.
- [9] J. Huang and K.A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on power electronics*, vol. 21, no. 1, pp.140-147, January 2006.
- [10] A.Nami, F.Zare, A. Ghosh and F.Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped h-bridge cells," *IEEE Transactions on power electronics*, vol. 26, no. 1, pp.51-65, January 2011.
- [11] G. Ceglia, V. Guzmán, C. Sánchez, F. Ibáñez, J. Walter, and M. I. Giménez, "A new simplified multilevel inverter topology for dc-ac conversion," *IEEE Transactions on power electronics*, vol. 21, no. 5, pp.1311-1319, September 2006.
- [12] G.-J. Su, "Multilevel DC-link inverter," *IEEE Transactions on industry applications*, vol. 41, no. 3, pp. 848-854, May/June 2005.
- [13] P. Rodriguez, M. D. Bellar, R. S. Muñoz-Aguilar, S. Busquets-Monge, and F.Blaabjerg, "Multilevel-clamped multilevel converters (MLC2)," *IEEE Transactions on power electronics*, vol. 27, no. 3, pp.1055-1060, March 2012.
- [14] N. D. Dao, and D-C. Lee, "Operation and control scheme of a five-level hybrid inverter for medium voltage motor drives," *IEEE Transactions on industrial electronics*, TPEL.2018.
- [15] K.K. Gupta, A. Ranjan, P. Bhatnagar, L. K.Sahu, and Sh. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Transactions on power electronics*, vol. 31, no. 1,pp. 135-151, January 2016
- [16] S. F. Kia, H. I. Eini and S.Farhangi , "Increasing the Number of Voltage levels in single-phase Multilevel Converters," *The 6th International Power Electronics Drive Systems and Technologies Conference (PEDSTC20 15)* 3-4 February 2015, Shahi Beheshti University, Tehran, Iran. 2015.
- [17] Z. Pan, F. Z. Peng, V. Stefanovic, and M. Leuthen "A diode-clamped multilevel converter with reduced number of clamping diodes," 2004 .
- [18] S. Singhai , A. Pandey and V. Singh, "New topology of asymmetrical multilevel inverter [15/29 level]," *International Conference on Current Trends Toward Converging Technologies*, Combatore , India. 2017.
- [19] S. G. Song, F. S. Kang, and S-J. Park, "Cascade multilevel inverter employing three-phase transformers and single dc input," *IEEE Transactions on industrial electronics*, vol. 56, no 6 , pp. 2005-2014, June 2009 .
- [20] M. Zolfaghar, E. Najafi, and S. Hasanzadeh, "A modified diode clamped inverter with reduced number of switches," *2018 9th Annual Power Electronic, Drive System and Technologies Conference (PEDSTC)*, 2018.
- [21] V. Blasko "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison method," *IEEE Transactions on industry applications*, vol. 33, no. 3, pp.756-764, May / June 1997.
- [22] H.Mondol, S. P. Biswas, K.Hosain, F.Samad, and W. Rahman, "A Novel single phase multilevel inverter topology with reduce number of switching elements and optimum the performance," *International conference on Electrical ,Computer and communications Engineering (ECCE)* , 7-9 February, 2019.