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algorithm for 2D-data array addition using digit-decomposition-plane representation

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Abstract. In this paper, optical scalable parallel and high-speed 2D data array adder for trinary signed-digit (TSD) number is proposed. The digit-decomposition-plane (DDP) coding method is used to represent the 2D TSD data arrays. The algorithm performs parallel TSD addition in constant time independent of the size of the TSD data arrays. The design describes methodology to involve two-step TSD adder. The TSD addition is expressed with several combination logic formulas that are newly derived. Optical implementation with classical optical elements is suggested for proposed TSD adder. Preliminary demonstration example is also described.

1- Introduction

Today, the world is in need to ultrahigh speed processing devices, to fulfill the theories of the new technologies that require very high speed. The electronic digital processing devices are developed to match these demands but they stay limited because the parallelism and high-speed of the digital systems are complex in implementation.

The new technology uses the light in large parts of the processing systems, and called "**Optical Computing Systems**" [1, 2].

The optical processing systems had been leaded to many advantages, which might needed for very high speed processing systems. The important advantage was the parallelism. The parallelism of optical processing systems was flexible and not complex in implementation, so data in one-dimension and multi-dimension can be processed [3].

In optical processing systems, the light signals can pass through each other without

12 interacting or influencing the data carried by.

This feature overcame the problem that named "*Von Neuman bottleneck*" in the digital computers. It gave a large communication links between processing units in a small area.

These optical techniques had been established using many parallel algorithms in order to perform the arithmetic operations. Some of these parallel algorithms used the redundant binary numbers [4]. The other used a multi-leveled number system based on residue arithmetic algorithm. Also, parallel optical logic gates had been suggested to process large amounts of data in parallel and in speed of light [5]. Carry-free full parallel optical one-step TSD adder using symbolic substitution (SS) technique is studied in [6]. Also, a receded TSD adder using SS technique had been presented in [7].

Recently, optical parallel scalable three-step modified signed-digit (MSD) adder for large-scale two 2D MSD data arrays coded by DDP representation had been studied [8]. Also, high speed parallel optical adder for QSD number using digit-decomposition-plane (DDP) representation is suggested in [9].

In this research, we propose a parallel digital addition algorithm to array calculation. The algorithm for addition of two n-digit $M \times N$ TSD data arrays will generate $M \times N \times (n+1)$ partial terms, where M is the number of rows and N is the number of columns, while n is the number of TSD digit per one number. The proposed techniques

perform parallel TSD addition in constant time, and are of great benefit to array calculation. The digit-decomposition-plane (DDP) coding method is used to represent the 2D TSD data arrays. DDP is used in this work because there are two apparent features of this coding method. The first one is that any DDP plane is the complement of the superimposing plane of the other planes. The superimposing plane is obtained by accumulated the bright and dark pixels in one plane. The second one is that if all DDP planes are superimposed, the result will be a totally transparent plane. The design describes methodology for obtaining two-step TSD adder. The TSD addition has been described with several combination logic formulas and then implemented using simple optical elements, such as beam splitters, mirrors, beam combiners, light sources array, and light detectors array. Various examples are performed in order to test computer simulation.

2 - TSD two-step adder

The two-step adder for TSD numbers is expressed according to the following two equations:

$$\text{Step 1: } x_i + y_i = 3c_i + s_i \quad (1)$$

$$\text{Step 2: } s_i + c_{i-1} = z_i \quad (2)$$

Figure. 1 presents the block diagram of this adder. Boxes D (first step) add the CP digits (x_i, y_i) of addend number X and

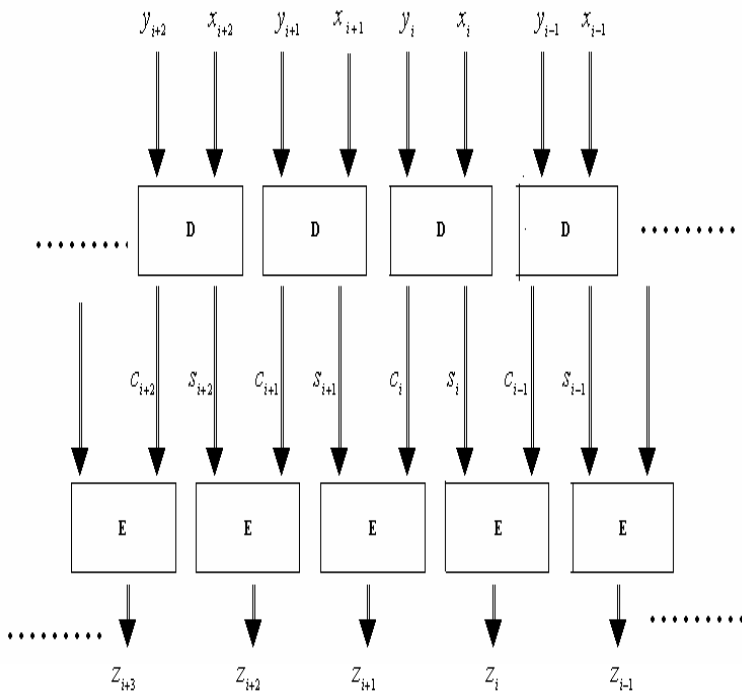


Fig. 1: Block diagram of two-step TSD adder, where the functional blocks D and E employ the TSD addition rules shown in Eqs. (1) and (2), respectively.

augend's number Y , which are both n -digit TSD numbers, to produce the intermediate sum and carry (s_i, c_i) according to the computational rules of Table 1-a. Boxes E (second step) add s_i to c_{i-1} , to obtain the final result z_i depending on computational rules of Table 1-b. First, the 25 combinations of $CP(x_i, y_i)$ can be classified into 9 groups ($G_1 - G_9$) [6]. Each group G_i represents one computational rule of the first step addition. Table 1-a considers these 9 rules in order to obtain s_i and c_i according to the values of

Table 1: Truth tables for TSD arithmetic

groups	current pair CP	intermediate results	
		s	c
G_1	(x, y)		
G_2	$(2, 2)$	1	1
G_3	$(2, 1), (1, 2)$	0	1
G_4	$(2, 0), (0, 2), (1, 1)$	$\bar{1}$	1
G_5	$(2, \bar{1}), (1, 0), (0, 1), (\bar{1}, 2)$	1	0
G_6	$(2, \bar{2}), (\bar{2}, 2), (1, \bar{1}), (\bar{1}, 1), (0, 0)$	0	0
G_7	$(\bar{2}, \bar{1}), (\bar{1}, 0), (0, \bar{1}), (1, \bar{2})$	$\bar{1}$	0
G_8	$(\bar{2}, 0), (0, \bar{2}), (\bar{1}, \bar{1})$	1	$\bar{1}$
G_9	$(\bar{2}, \bar{1}), (\bar{1}, \bar{2})$	0	$\bar{1}$
G_{10}	$(\bar{2}, \bar{2})$	$\bar{1}$	$\bar{1}$

(a)

groups	intermediate results	final results
H_1	(s, c)	
H_2	$(1, 1)$	2
H_3	$(1, 0), (0, 1)$	1
H_4	$(1, \bar{1}), (\bar{1}, 1), (0, 0)$	0
H_5	$(\bar{1}, 0), (0, \bar{1})$	$\bar{1}$
H_6	$(\bar{1}, \bar{1})$	$\bar{2}$

(b)

the two digits of the i -th CP. Also, In Table 1-a, it is clear that each s_i and c_i has only three TSD weights $\{1, 0, \bar{1}\}$, so there are 9 combinations of (s_i, c_{i-1}) can be classified into 5 groups ($H_1 - H_5$) as shown in Table 1-b to represent the computational rules of the second step addition. So, the final result will be $(n+1)$ -digit TSD number.

3- TSD addition with DDP representation

DDP representation had been proposed by *Hongxin Huang* and *et.al* [8]. It is an extension for bit-plane representation method.

DDP representation can be applied to code large 2D data arrays of TSD numbers. The 2D TSD numbers data array can be coded using DDP representation in 5 DDP planes (DDP- 2, 1, 0, $\bar{1}$, $\bar{2}$). Figure 2 shows example for TSD data array coded by DDP scheme. The addend A and augend's B $M \times N \times n$ TSD arrays will be decomposed into 5 DDP planes for each one, they are ($A_2, A_1, A_0, \bar{A}_1, \bar{A}_2$ and $B_2, B_1, B_0, \bar{B}_1, \bar{B}_2$).

Two steps are used to derive the logical formulas in order to implement TSD adder.

• **First-step:**

In Table 1-a, the intermediate sum S_i will be 1 if the following rule is succeeded:

$$IF (x_i, y_i) = (2,2)OR(2,\bar{1})OR(1,0)OR(0,1)OR(\bar{1},2)OR(\bar{2},0)OR(0,\bar{2})OR(\bar{1},\bar{1}) THEN s_i = 1 \quad (3)$$

X_i and y_i equal to 2,1,0, $\bar{1}$, and $\bar{2}$ digits are separated and decomposed to the (j,i)-th pixels of A and B DDP planes. Then, equation (3) can be rewritten as:

$$s1_{ji} = a2_{ji} * b2_{ji} + a2_{ji} * \bar{b1}_{ji} + a1_{ji} * b0_{ji} + a0_{ji} * b1_{ji} + a\bar{1}_{ji} * b2_{ji} + a\bar{2}_{ji} * b0_{ji} + a0_{ji} * \bar{b2}_{ji} + a\bar{1}_{ji} * \bar{b1}_{ji} \quad (4)$$

The plane S1 (DDP-1 plane) of the intermediate sum array S can be obtained in parallel depending on the following rule:

$$\begin{bmatrix} 15 \\ -52 \\ -22 \\ 4 \end{bmatrix}_{111} = \begin{bmatrix} 0120 \\ i\bar{2}\bar{2}i \\ i\bar{1}\bar{2}2 \\ 0011 \end{bmatrix}_{111}$$

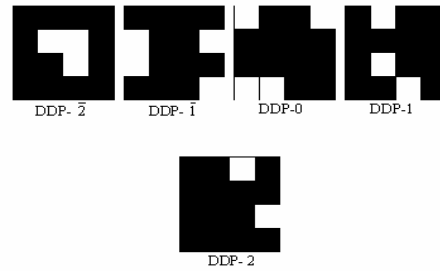


Fig. 2 : Optical DDP coding of TSD data array

$$S1 = A2 * B2 + A2 * \bar{B1} + A1 * B0 + A0 * B1 + A\bar{1} * B2 + A\bar{2} * B0 + A0 * \bar{B2} + A\bar{1} * \bar{B1} \quad (5)$$

This can be simplified to:

$$S1 = (A2 + A\bar{1}) * (B2 + \bar{B1}) + A0 * (B1 + \bar{B2}) + (A1 + A\bar{2}) * B0 \quad (6)$$

The intermediate sums and carries of all adding numbers included in A and B arrays will be generated in parallel in six DDP planes ($S1, S0, \bar{S1}$ and $C1, C0, \bar{C1}$). In the same way of obtaining S1 plane, the rest five DDP planes can be also obtained from Table 1-a.

$$\bar{S1} = (A1 + A\bar{2}) * (B1 + \bar{B2}) + A0 * (B2 + \bar{B1}) + (A2 + A\bar{1}) * B0 \quad (7)$$

$$S0 = (A2 + A\bar{1}) * (B1 + \bar{B2}) + (A1 + A\bar{2}) * (B2 + \bar{B1}) + A0 * B0 \quad (8)$$

$$C1 = (A2 + A1) * (B2 + B1) + A2 * B0 + A0 * B2 \quad (9)$$

$$\bar{C1} = (\bar{A1} + \bar{A2}) * (\bar{B1} + \bar{B2}) + \bar{A2} * \bar{B0} + \bar{A0} * \bar{B2} \quad (10)$$

$$C0 = (A2 + A1) * (\bar{B1} + \bar{B2}) + (\bar{A1} + \bar{A2}) * (B2 + B1) + A0 * (B1 + \bar{B1})(A1 + A0 + \bar{A1}) * B0 \quad (11)$$

• Second-step:

Table 1-b shows the computational rules of the second-step in two-step TSD adder. Simply, the logical formulas of the second-step can be derived from the $S1$, $S0$, $\bar{S1}$, $C1$, $C0$, and $\bar{C1}$ planes which are generated in the first-step. The first rule in the Table 1-b is:

$$IF (s_i, c_{i-1}) = (1,1) \text{ THEN } z_i = 1 \quad (12)$$

Similar from the first-step phase, we can get the five TSD DDP planes of the final results $Z2$, $Z1$, $Z0$, $\bar{Z1}$, and $\bar{Z2}$ according to the following rules:

$$Z2 = S1 * C'1 \quad (13)$$

$$Z1 = S1 * C'0 + S0 * C'1 \quad (14)$$

$$Z0 = S1 * C'1 + S0 * C' + \bar{S1} * C'1 \quad (15)$$

$$\bar{Z1} = \bar{S1} * C'0 + S0 * C'1 \quad (16)$$

$$\bar{Z2} = \bar{S1} * C'1 \quad (17)$$

The $M \times N \times n$ TSD array A is added with the $M \times N \times n$ TSD array B in parallel and will

generate the $M \times N \times (n+1)$ TSD array which is presented the final results, and indicated by planes $Z2$, $Z1$, $Z0$, $\bar{Z1}$, and $\bar{Z2}$.

4- Optical implementation

The optical hardware schemes of this parallels TSD array adder can be implemented practically using simple optical tools. The logical AND and OR are the main operations in the logical formulas. The principles handled for AND and OR operations will be considered to realize our suggestion for TSD adder [5, 8]. Logical AND can be achieved optically by cascading two DDP planes, each of one array, with same dimensions and pixel resolutions. The light beams will be applied on each pixel of the first plane. These beams will pass through the transparent pixel (1) and blocked by opaque pixel (0). Thereby, four combinations of transparent (1) and opaque (0) pixels of the two DDP planes will be presented: (1×1) , (1×0) , (0×1) , and (0×0) . Only in case (1×1) the light beam will pass through the two cascaded planes. So, this optical AND can process $M \times N \times n$ binary AND operations in parallel. Fig. 3 shows the optical implementation of the logical AND. a pixel-wise addition in parallel for the corresponding Optical logical OR can be realized using beam combiner (BC). BC performs light beams of the two packages passed through two DDP planes and fallen onto the two BC input surfaces. Three pixel-wise addition cases will be gain: $(1+0)$, $(0+1)$, and $(0+0)$.

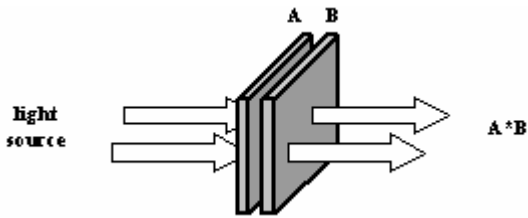


Fig. 3: AND gate optical implementation

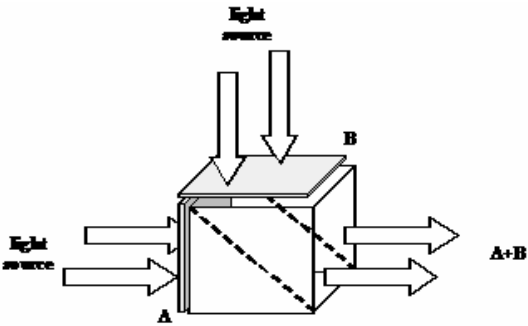


Fig. 4: OR gate optical implementation

The case (1+1) will never appear because the pixel-wise addition is done between two DDP planes of the same array. So, $M \times N \times n$ binary OR operations will be done in parallel. Fig. 4 illustrates the optical implementation of the logical OR.

The proposed parallel optical two-step TSD adder operation can be explained as following:

- 1- The input $M \times N \times n$ DDP-planes of the first step will be illuminated by Laser sources to enter the optical system for processing.
- 2- Light detector arrays (LDAs) in the end of optical scheme of the first step will detect the DDP-planes of the intermediate results that produced by the first step.
- 3- These optical signals will be converted to electrical signals and passed to the optical implementation of the second step.


4- The input DDP-planes of the second step will be addressed in parallel by these electrical signals to form the sufficient expanded and shifted copies of the intermediate results. Expanding and shifting means that, one pixel is necessary to be padded to the LSB and MSB pixel position of the detected DDP-planes of the intermediate carry and intermediate sum, respectively.


5- Finally, the LDAs will detect the optical signals that represent the DDP-planes in the final result array, which will be $M \times N \times (n+1)$ TSD array.


The above points will present the complete optical implementation of the suggested parallel optical two-step TSD adder with the consideration of the following explanations:

BC : denotes a beam combiner.

BS : denotes a beam splitter.

 : denotes a mirror.

 : denotes SLM (DDP plane),
LDA, or CMP.

 : the direction of the light
signal emitted by an optical
source.

The optical implementation of the two steps 2D TSD array is shown in Fig. 5.

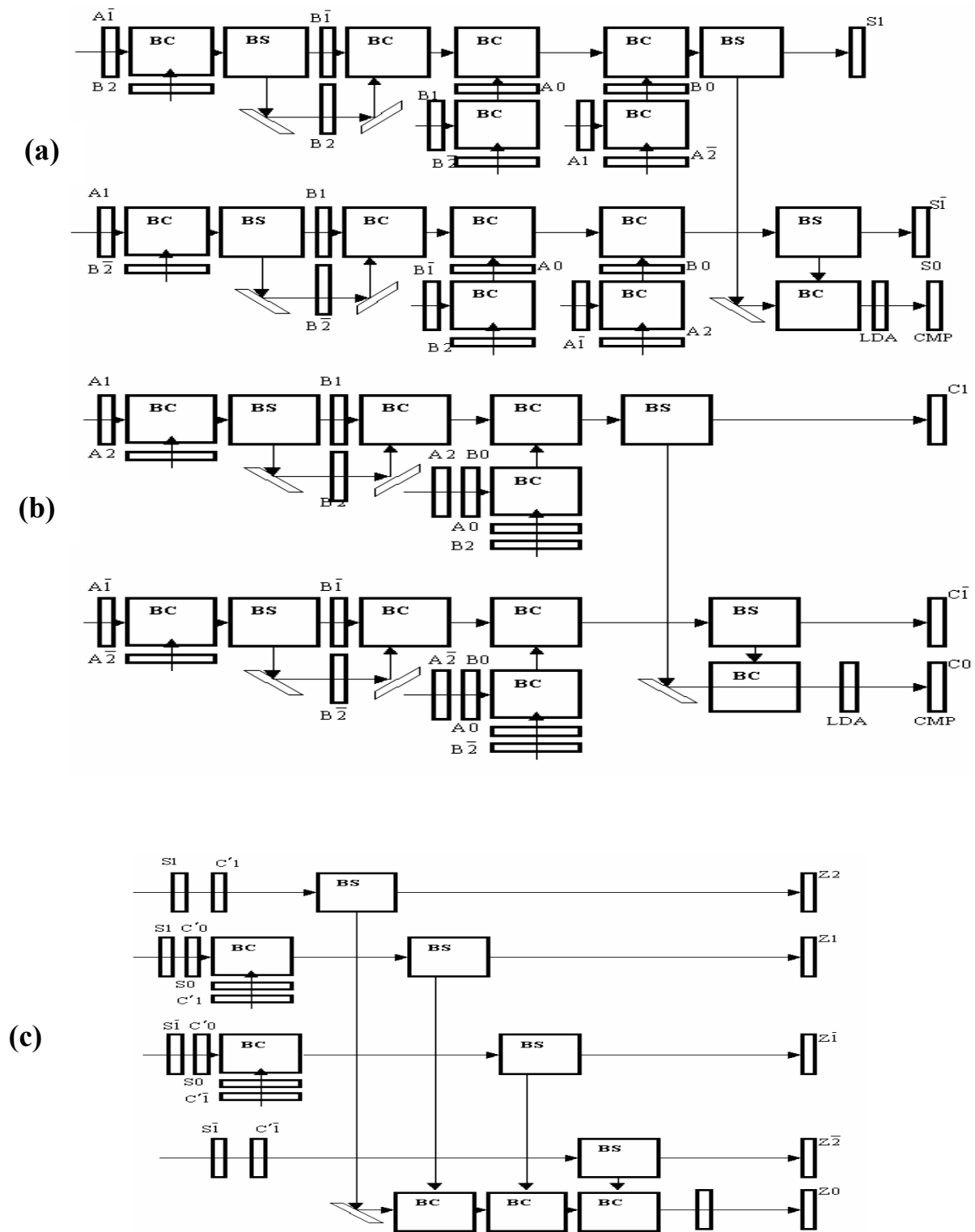


Fig. 5: Optical implementation of the 2D –data array TSD adder
(a): First-step, (intermediate sum generation).
(b): First-step, (intermediate carry generation).
(c): Second-step, (final results generation).

$$A = \begin{bmatrix} 80 & 77 \\ -21 & 42 \\ 37 & 11 \\ 20 & -80 \\ 33 & 74 \\ 18 & -32 \\ -30 & -11 \\ 2 & 22 \\ 43 & -14 \\ 78 & 51 \end{bmatrix}_{10} = \begin{bmatrix} 2222 & 2212 \\ 0\bar{2}\bar{1}0 & 1120 \\ 1101 & 0102 \\ 0202 & \bar{2}\bar{2}\bar{2}\bar{2} \\ 1020 & 2202 \\ 0200 & 10\bar{1}\bar{2} \\ \bar{1}0\bar{1}0 & 0\bar{1}0\bar{2} \\ 0002 & 0211 \\ 1121 & 0\bar{1}\bar{1}\bar{2} \\ 2220 & 1220 \end{bmatrix}_{TSD}$$

$$B = \begin{bmatrix} 80 & 35 \\ 53 & 11 \\ -57 & -75 \\ 79 & -9 \\ -33 & -14 \\ 28 & -65 \\ -70 & 53 \\ 7 & -77 \\ 14 & -43 \\ -55 & -23 \end{bmatrix}_{10} = \begin{bmatrix} 2222 & 1022 \\ 1222 & 0102 \\ \bar{2}0\bar{1}0 & \bar{2}\bar{2}\bar{1}0 \\ 2221 & 0\bar{1}00 \\ \bar{1}0\bar{2}0 & 0\bar{1}\bar{1}\bar{2} \\ 1001 & \bar{2}\bar{1}0\bar{2} \\ \bar{2}\bar{1}\bar{2}\bar{1} & 1222 \\ 0021 & \bar{2}\bar{2}\bar{1}\bar{2} \\ 0112 & \bar{1}\bar{1}\bar{2}\bar{1} \\ \bar{2}00\bar{1} & 0\bar{2}\bar{1}\bar{2} \end{bmatrix}_{TSD}$$

$$Z = \begin{bmatrix} 12221 & 11011 \\ 0102\bar{1} & 0200\bar{1} \\ 0\bar{1}\bar{1}\bar{1} & \bar{1}\bar{1}\bar{1}0\bar{1} \\ 10200 & \bar{1}0\bar{1}01 \\ 00000 & \bar{1}\bar{1}\bar{1}\bar{1}0 \\ 0\bar{2}\bar{1}01 & \bar{1}0\bar{1}\bar{2}\bar{1} \\ \bar{1}0\bar{2}0\bar{1} & 01\bar{2}\bar{1}0 \\ 00100 & \bar{1}\bar{1}00\bar{1} \\ 02010 & 0\bar{2}0\bar{1}0 \\ 010\bar{1}\bar{1} & 01001 \end{bmatrix}_{TSD} = \begin{bmatrix} 160 & 112 \\ 32 & 53 \\ -20 & -64 \\ 99 & -89 \\ 0 & 60 \\ 46 & -97 \\ -100 & 42 \\ 9 & -55 \\ 57 & -57 \\ 23 & 28 \end{bmatrix}_{10}$$

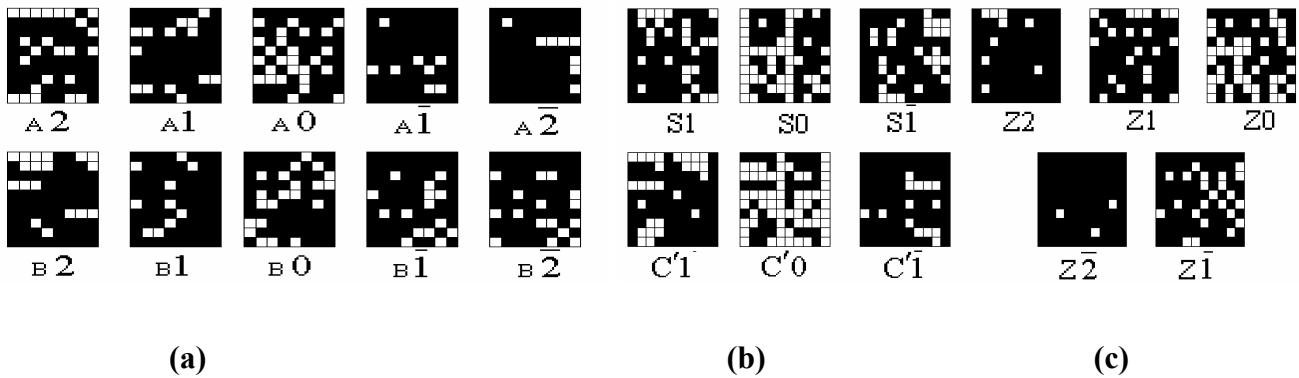


Fig. 6: Simulation results of the two-step 2D-data array TSD adder.

- (a) A and B SLM inputs.
- (b) First-step intermediate Sum and Carry generations.
- (c) Second-step (final results generations).

5- Simulation results

The computer program using C++ language is used to simulate the optical implementation of the proposed TSD adder. This program is built and executed for two-step TSD adder using DDP representation. The two $10 \times 2 \times 4$ TSD arrays A and B will be used to test the operation of the proposed TSD array adder. Figure 6 shows the DDP-planes of the two TSD arrays A and B. The First-step intermediate Sum and intermediate Carry generations are presented in Fig. 6-b. While the final results are shown in Fig. 6-c.

6- Conclusions

In this work, the parallel scalable optical two-step TSD adder is proposed. The $M \times N \times n$ TSD data arrays are processed using the apparent features of the DDP coding method. Computer programming is used to simulate the logical formulas of the TSD adder. Practical example is discussed and verified by computer simulations. It is found that the simulation results are confidence, and that the newly technique is performed correctly. Simple classical optical tools are suggested successfully to implement this TSD adder. Tools like AND gate, OR gate, BS,

BC, LDA, CMP, SLM, and mirrors are used to constructed TSD adder.

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