Control of ZCZVT Commutation Cell Inverter

Rabee' Hashim Thejel
Department of Electrical Engineering-College of Engineering-
University of Basrah

Abstract

This paper proposes a new control circuit to control the switching of the main switches of the used Zero Current Zero Voltage Transition (ZCZVT) inverter to ensure Zero Current and Zero Voltage Switching (ZCZVS). The reverse recovery losses of the main diodes are minimized and the auxiliary switches of the commutation cell are turned on at Zero Current Switching (ZCS) and off at ZCZVS. The commutation losses are practically reduced to zero due to ZCS. Sinusoidal Pulse Width Modulation (SPWM) is used to perform the switching of the power semiconductor devices and to control the output voltage value. MATLAB software is used to simulate the inverter circuit. Simulation results are presented to demonstrate the feasibility of the proposed control circuit.

السيطرة على مبدل ذو خلية اطفاء نوع ZCZVT

ربيع هاشم تجيل / قسم الهندسة الكهربائية – كلية الهندسة – جامعة البصرة

الخلاصة

يعرض هذا البحث دائرة سيطرة جديدة للسيطرة على قدح المفاتيح الرئيسة للمبدل نوع (ZCZVT) المستخدم لضمان حصول القدح عند تيار وفولتية مساويان للصفر (ZCZVS). مفقودات الاسترداد العكسي للثنائيات الرئيسة تم خفضها والمفاتيح الثانوية لخلية الإطفاء يتم تشغيلها عند تيار مساوي للصفر (ZCS) وإطفائها عند تيار وفولتية مساويان للصفر (ZCZVS). مفقودات الإطفاء انخفضت عمليا بسبب الإطفاء عند تيار مساوي للصفر. استعملت طريقة تضمين عرض النبضة الجيبي (SPWM) لأجراء عملية قدح المفاتيح والتحكم بقيمة فولتية الاخراج. تم استعمال برامجيات MATLAB لتمثيل دائرة المبدل. النتائج المستعرضة لهذا التمثيل تبين صلاحية دائرة السيطرة المقترحة.

1.Introduction

With the growing development of power devices technology, switching mode power conversion moves toward high frequency operation. For inverters, the operation at high frequency is required to reduce the audible noise, the volume and weight of filters, as well as to improve output voltage quality[1,2,3].

Several previous publications have resorted to hard switching techniques for inverters[4,5]. These techniques suffer from high switching stresses produce by the overlapping of voltage and current result in high switching losses. Whereas, soft switching commutation of power semiconductor devices aims to reduce the switching losses, enables high frequency operation and achieving high power density[2]. Some efforts have been made to reach these aims and various topologies were proposed to achieve soft switching in voltage source inverters[1,2,3,6,7,8].

The quasi-parallel resonant DC link inverter was proposed to perform the conversion to achieve the soft switching action. In this inverter, the voltage stresses of the inverter switches can be clamped to the value of the voltage source due to the action of soft switching. By the adjustment of the on/off instants of the switching devices and the adequate choice of the related components, the system can

have no snubber and operate in high frequency[6].

A regenerative passive snubber circuit for pulse width modulation inverters to achieve soft switching purposes with significant cost and reliability penalties was presented. This passive soft-switching snubber employs a diode/capacitor snubber circuit for each switching device in an inverter to provide low dv/dt and low switching losses to the device[8].

A new ZCZVT commutation cell for PWM DC-AC converters was proposed[2]. The used commutation cell allows the main switches to be turned on and off at zero current and zero voltage (ZCZVS). The auxiliary switches are turned on at ZCS and off at ZCZVS.

In the Present work a new control circuit is proposed to control this ZCZVT inverter. This circuit combines the goals of soft switching commutation for all active switches and sinusoidal pulse width modulation (SPWM) strategy to control the AC output voltage. The use of SPWM strategy is very effective in keeping the generated harmonics beyond the bandwidth of the system being activated and therefore these harmonics do no dissipate power[9]. The important feature of the present control circuit among the previously mentioned methods that it exactly detects the correct period of soft switching of the active switches through continuosly monitoring the switch-shunting diode current signal.

2. Principles of Operation

The overall inverter circuit is simulated using MATLAB simulink computer software.

2.1 The ZCZVT SPWM Full-Bridge Inverter

Fig.1 shows the ZCZVT SPWM full-bridge inverter. It differs from a hard-switching SPWM full-bridge inverter by the presence of an additional shunt resonant network composed of two resonant capacitors C_{R1} and C_{R2}, two resonant inductors L_{R1} and L_{R2}, and two bi-directional auxiliary switches S_{A1}-D_{A1} and S_{A2}-D_{A2}. Insulated Gate Bipolar Transistors (IGBTs) are used for the main and auxiliary switching devices.

There are sixteen operation stages during one switching cycle[2]. The proper switching of the auxiliary switches allows the main switches commutations to happen simultaneously with zero voltage and zero current

Semiconductor switching devices S_1 and S_4 of the main circuit and S_{A1} of the auxiliary circuit are controlled through the positive half cycle. While, S_2 and S_3 of the main circuit and S_{A2} of the auxiliary circuit during the negative half cycle.

2.2 Inverter Control Circuit

The block diagram of the proposed circuit is shown in Fig.2.

This circuit composed of

1. Sinusoidal pulse width modulation circuit.
2. Primary switching-pulses generator.
3. Current signal-to-pulses conversion circuit.
4. Final ZCZVS shaping circuit.

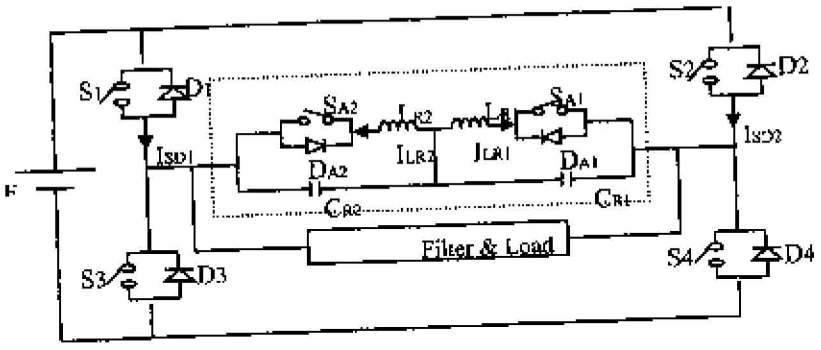

Fig.1 ZCZVT SPWM full-bridge inverter.

2.2.1 Sinusoidal Pulse Width Modulation (SPWM) Circuit

Sinusoidal PWM techniques are one of the most popular modulation methods in industrial applications. This method involves a comparison of the reference input, which is basically is a sinusoidal waveform with V_s amplitude, against a triangular carrier waveform and detection of cross over instances determine switching events. Fig.3 shows the parts of this circuit. The voltage-controlled oscillator (VCO) generates sinusoidal voltage with F_s frequency and unity voltage amplitude. The triangular generator generates triangular voltage with F_r frequency and V_r voltage amplitude. Fig.4 shows the generation of the SPWM pulses. In this figure, the pulses SPWMP are used to generate the inverter firing pulses during the inverter positive half cycle operation, while SPWMN are during the negative half cycle.

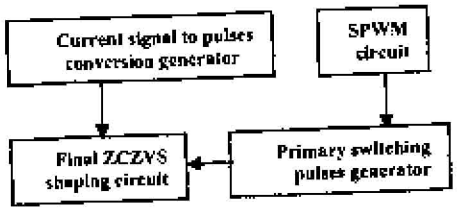

Fig.2 The proposed control circuit.

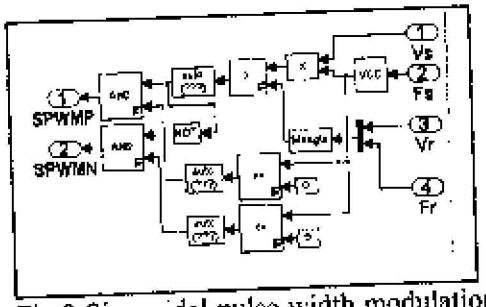

Fig.3 Sinusoidal pulse width modulation circuit.

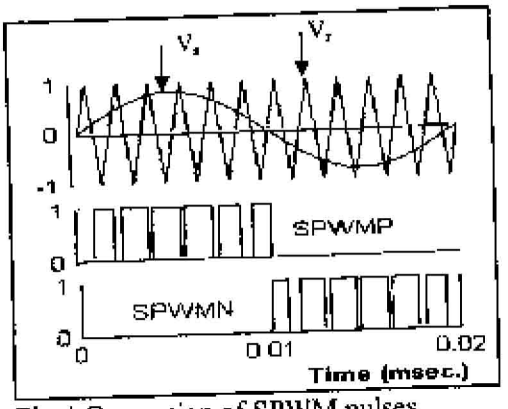

Fig.4 Generation of SPWM pulses

2.2.2 Primary Switching-Pulses Generator Circuit

This circuit consists of two identical parts. One works during the inverter positive half cycle while the other during the negative half cycle. The first part, shown in Fig.5, treats the pulses formed by the SPWM circuit (SPWMP pulses) to generate the switching pulses of the main and auxiliary switches as a primary stage as illustrated in Fig.6.

These primary pulses are G14i, GSA1P, and GSA1N. Where,

G14i is the primary switching pulses of the main switches S_1 and S_4.

GSA1P is the primary switching pulses of the auxiliary switch S_{A1} which will initiate the soft on operation of the main switches S_1 and S_4.

GSA1N is the primary switching pulses of the auxiliary switch S_{A1} which will initiate the soft commutation of the main switches S_1 and S_4.

2.2.3 Current-to-Pulses Conversion Circuit

This circuit converts part of the negative portion of the anti-parallel switching transistor-diode current signal, the shunting diode current signal, to pulses for all power semiconductor switching-devices. This circuit consists of four identical parts to perform the conversion for I_{LR1}, I_{LR2}, I_{SD1}, and I_{SD2} currents. One of these parts is illustrated in Fig.7. The operation of this circuit is shown in Fig.8.

2.2.4 Final ZCZVS shaping Circuit

This circuit consists of four parts. Two identical parts are used to formulate the final switching pulses for S_{A1} and S_{A2} auxiliary switching devices. Another two identical parts are used to formulate the final ZCZV switching pulses, one for S_1 and S_4 and the other for S_2 and S_3

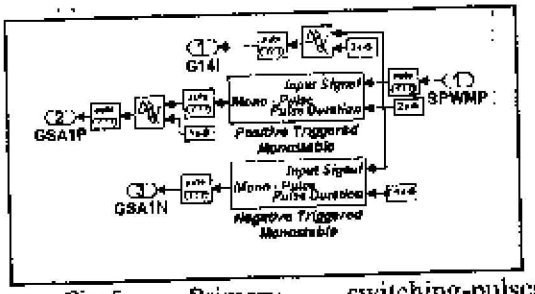

Fig.5 Primary switching-pulses generator circuit

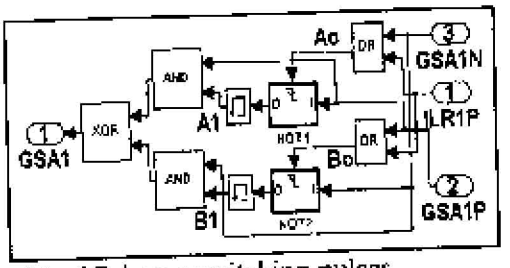

Fig.6 Primary switching-pulses.

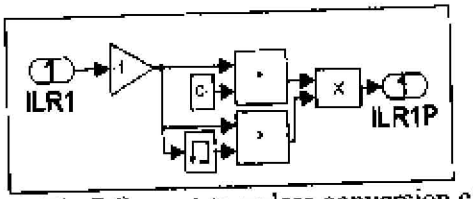

Fig.7 Current-to-pulses conversion circuit

The first part, which generates the firing pulses of the auxiliary switch

S_{A1}, is shown in Fig.9. This circuit logically treats the pulses ILR1P, GSA1P, and GSA1N to generate GSA1 pulses. These logical treatments can be summarized as follows:

$Ao=GSA1N+ILR1P$ .....(1)

$Bo=GSA1P+ILR1P$ .....(2)

$A1=\overline{GSA1P}\downarrow Ao$ .....(3)

$B1=\overline{GSA1N}\downarrow Bo$ .....(4)

$GSA1=A1.GSA1P \oplus B1.GSA1N$ ...(5)

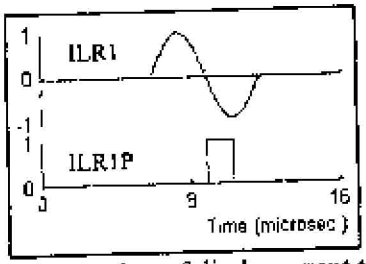

Fig.8 Conversion of diode current to pulse.

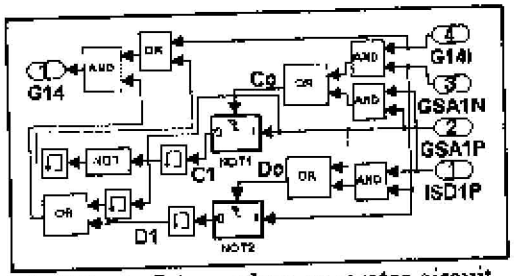

Fig.9 S_{A1}'s firing pulses generator circuit.

It is clear from Eq.(3) that A1 is the complement of GSA1P. This complement becomes available only under the negative edge trigger of Ao pulse. Fig.10 shows the generation of these pulses. This figure proves clearly that the auxiliary switch S_{A1} is turned on at ZC and off at ZCZV, i.e., during the conduction of S_{A1} shunting diode. Similar circuit is used to switch S_{A2}

The third part, shown in Fig.11, is used to control S_1 and S_4 switching. The pulses ISD1P, G14i, GSA1P, and GSA1N are logically treated to formulate the final pulses for GSA1 pulses, these logical treatments can be given as:

$Co=G14i.GSA1N+ISD1P.GSA1P$ .....(6)

of the main switches S_1 and S_4. Also, as done

$Do=ISD1P.GSA1N+GSA1P$ ...(7)

$C1=GSA1P \quad Co$ .....(8)

$D1=\overline{GSA1N}\downarrow Do$ .....(9)

$G14=(G14i+C1).(GSA1P+D1)$ .....(10)

In the generation of G14 pulses, ZCZV switching is completely satisfied during on and off conditions of the switches (see Fig.12). Similar procedures are carried out for the main switches S_2, S_3.

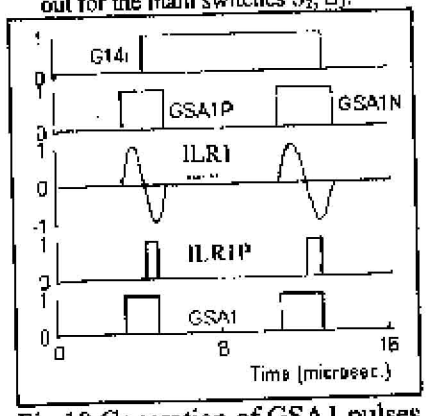

Fig.10 Generation of GSA1 pulses

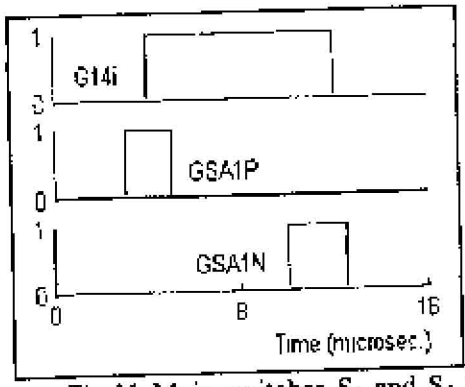

Fig.11 Main switches S_1 and S_4 firing-signals generator

Table-1 Components and parameters of the used inverter.

Component	Parameter
Input voltage (E)	200 V
Output power (P_o)	1000 W
Output voltage (V_o)	110 Vrms.
L_{R1} and L_{R2}	2.4 μH
C_{R1} and C_{R2}	34.7 nF
L (output filter)	2 mH
C (output filter)	100 μF
Load (R)	12Ω
Output frequency (F_s)	50 Hz
Switching frequency (F_c)	30 KHz

3. Simulation Results and Observations

The complete proposed inverter circuit is shown in Fig.13. This circuit has been implemented using MATLAB computer software. The components and parameters used are summarized in Table-1. The parameters of the commutation cell (L_{R1}, L_{R2}, C_{R1}, and C_{R2}) are calcultated using the following equations[1,2]

$$\omega I_o=\frac{\sqrt{2}P_o}{V_o}(1+\Delta I) \qquad \ldots\ldots(11)$$

$$Z_o=\frac{E}{\sqrt{2}KI_o} \qquad \ldots\ldots(12)$$

$$=\frac{\frac{di}{dt}\sqrt{2}\mathrm{Sin}^{-1}(1/2k)}{I_o} \qquad \ldots\ldots(13)$$

$$L_{R1}=L_{R2}=Z_o/\omega \qquad \ldots\ldots(14)$$

$$C_{R1}=C_{R2}=1/(Z_o\omega) \qquad \ldots\ldots(15)$$

Where:
I_o=The output peak current.
ΔI=The output current ripple, it is taken to be 20%.
Z_o=The characteristic impedance
S_1 and S_4 occurs truly without losses,i.e., with ZCZVS. In this figure, IS1 is the current through switch S_1, ID1 is the D_1 current, and VS1 is the voltage across switch S_1. Fig.15 shows that the auxiliary switch S_{A1} is turned on at ZCS and turned off at ZCZVS. Similar results can be obtained during the negative half cycle. Fig.16 shows the output voltage of the inverter after the LC filter. The output voltage distortion can be minimized by using modified PWM (SPWM) with a closed loop operation. Fig.17 shows the variation of the output voltage of the inverter with the variation of the sinusoidal voltage amplitude (V_s) of the used SPWM. This figure proves that the inverter output voltage can be controlled successfully through V_s adjustment.

4. Conclusions

A new control circuit for a ZCZVT full-bridge SPWM inverter has been proposed in this paper. The simulation results presented verify the validity of this scheme. These results show that the theoretical goals of ZCZVS for the main switches and ZCS at on states and ZCZVS at off states for the auxiliary switches are proved. This means that there is no voltage and current stresses on the power semiconductor devices and

the commutation losses are reduced to minimum.

References

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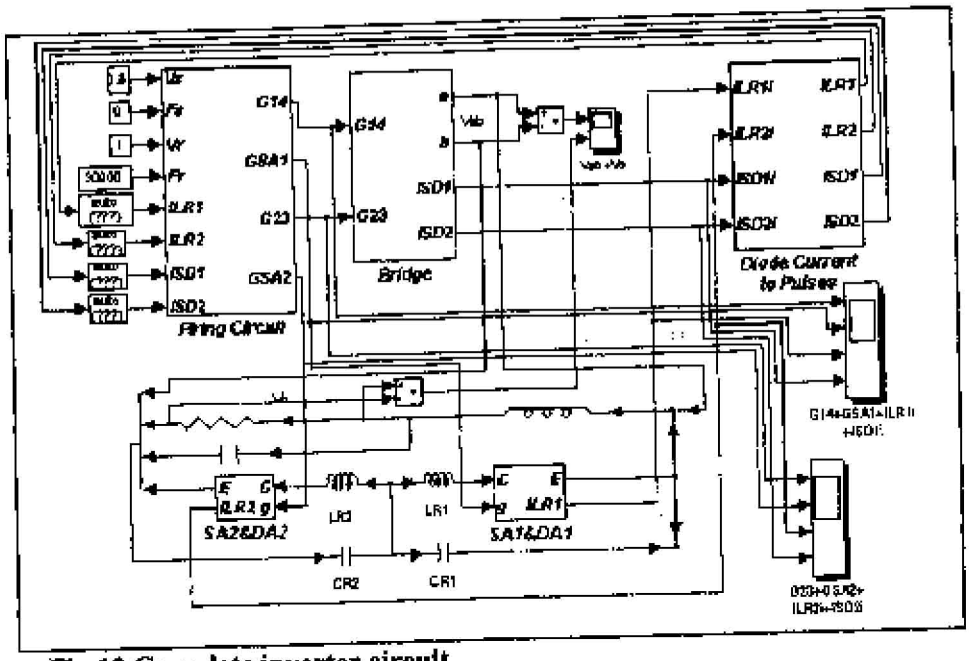

Fig.13 Complete inverter circuit.

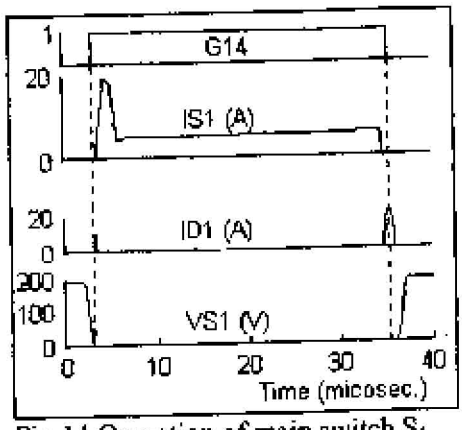

Fig.14 Operation of main switch S_1.

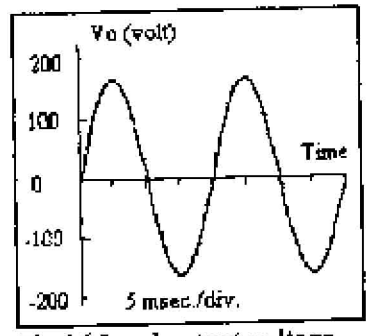

Fig.16 Load output voltage.

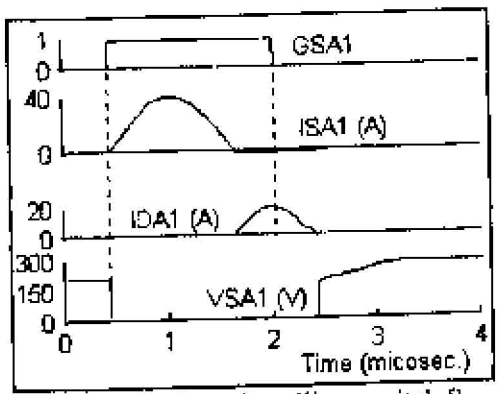

Fig.15 Operation of auxiliary switch S_{A1}.

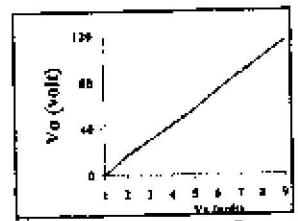

Fig.17 Variation of output voltage with V_s.