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Proposed Topology for Voltage Sag Mitigation with New Control Strategy

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Abstract *voltage sags represent the greatest threat to the sensitive loads of industrial consumers, the microprocessor based-loads, and any electrical sensitive components. In this paper, a special topology is proposed to mitigate deep and long duration sags by using a modified AC to AC boost converter with a new control method. A boost converter is redesigned with a single switch to produces an output voltage that is linearly proportional to the duty cycle of the switch. On the other hand, the proposed control system is based on introducing a mathematical model that relates the missing voltage to the duty cycle of the boost converter switch. The simulation results along with the system analysis are presented to confirm the effectiveness and feasibility of the proposed circuit.*

***Index Terms*— Voltage sag, Dynamic voltage restorer (DVR), Series connected device (SD), AC-AC boost converter.**

I. INTRODUCTION

About 92% of power quality voltage problems such as transient and momentary interruptions that occur in the distribution power systems are attributed to voltage sags [1]. The voltage sags is very influential to sensitive loads, and voltage sag with 0.25 second is enough to interrupt the protection devices of the load [2],[3]. Voltage sags are classified according to their depth (between 10% and 90% of the rated nominal voltage) and the duration time of the sag that may take half cycle up to one minute according to IEEE std. and IEC std.1995 [4],[5]. This problem should be treated with great interest and find a proper method to mitigate its effects on the distribution system.

There are many power devices proposed to compensate voltage sags for sensitive loads as in [6], [7]. These devices contain series connected components to compensate the voltage sag by injecting the value of the missing voltage into the grid [8]. Many types of series connected device (SD) topologies are categorized according to their complexity, cost, and compensation capability. Dynamic-Voltage- Restorer (DVR) is one of widely and commonly used SD, and there are several kinds of DVR [9] that some of them use a series transformer which is not economic for long time sags due to their bulky size and high cost [10]. Transformerless SD topologies are presented to compensate the long time sags because of their small size, low cost, and light weight. Transformerless topologies includes, but not limited to, Dynamic Sag Corrector (DYSC), Active Voltage Quality Regulator with Parasitic Boost Circuit (PB-AVQR) and Simplified of PB-AVQR (SPB-AVQR) which represents a modified version of PB-AVQR topology [11], [12]. In addition to that, there are many control methods used to obtain the desired value of the duty-cycle such as PI controller method [13], predictive and dead-beat controller [14], discrete state space control method [15], [16], self-tuned fuzzy control method [17], [18], and neural network controller as in [19], [20].

In this paper, a proposed topology for voltage sag mitigation with new control strategy is presented. A boost converter with a single switch is modified and developed to deliver an output voltage that only depends on the duty cycle of the switch. Furthermore, an LC low pass filter is attached to the output of the modified boost converter to produce pure sinusoidal voltage wave.

The new control method is performed depending on proposing a mathematical model
that connects the value of the voltage gain with the duty cycle of the transistor switch. Another mathematical model that relates the duty cycle with input voltage of the pulse width modulation firing circuit is introduced too. The simulation results reveal that the proposed system can reasonably compensate long time sag with sag depth values approaching up to 70%.

II. Modified AC –AC Boost Converters

When a voltage disturbance is detected, the AC-AC boost converter should be controlled to inject the missing voltage in series with the supply voltage. There are several types of AC-AC boost circuit, some of them with two switches such as Dynamic Sag Corrector (Dysc), Active Voltage Quality Regulator with Parasitic Boost circuit PB-AVQR, and SPB-AVQR which are detailed in [11], [12]. In addition, some boost converters use one switch in their conversion process [21] which can increase the supply voltage approximately up to twice . By modifying the topology proposed in [21], the supply voltage can be increased to three times the input voltage by using two freewheeling diodes instead of five and different energy storing element values. Unlike the original design, the modifications also provide an output voltage depending only on the duty cycle of the switch. Moreover, to obtain a pure sinusoidal signal at the boost converter output, a suitable low pass filter has been attached to the output of the boost converter as shown in Fig. 1.

a. Operating Principles

In order to understand the operating principles of the proposed topology, Fig. 2 and 3 illustrate the different operating modes during the positive and negative half cycles of the supply voltage, respectively. In Fig. 2 and 3 the solid lines refer to the direction of the current flowing. When the transistor is switched ON as shown in Fig. 2(a) (which illustrates the operation during the positive half cycle), the supply charges the inductor L1, so the current passes through (L1, D2, D3). During this mode, the capacitor (C) discharges to maintain the load-voltage. When the transistor is switched OFF, as in Fig. 2(b), the capacitor will be charged from the energy stored in the inductor through the diode (D5). For the operating conditions in the negative half cycle, when the transistor is switched ON as shown in Fig. 3(a), the inductor (L1) is reversely charged. Besides, the capacitor (C) will compensate the load voltage. In adverse, the capacitor will be charged from the energy stored in inductor (L1), when the transistor is switched OFF as in Fig. 3(b). Therefore, in every half cycle of supply voltage the capacitor is discharged to provide the energy that

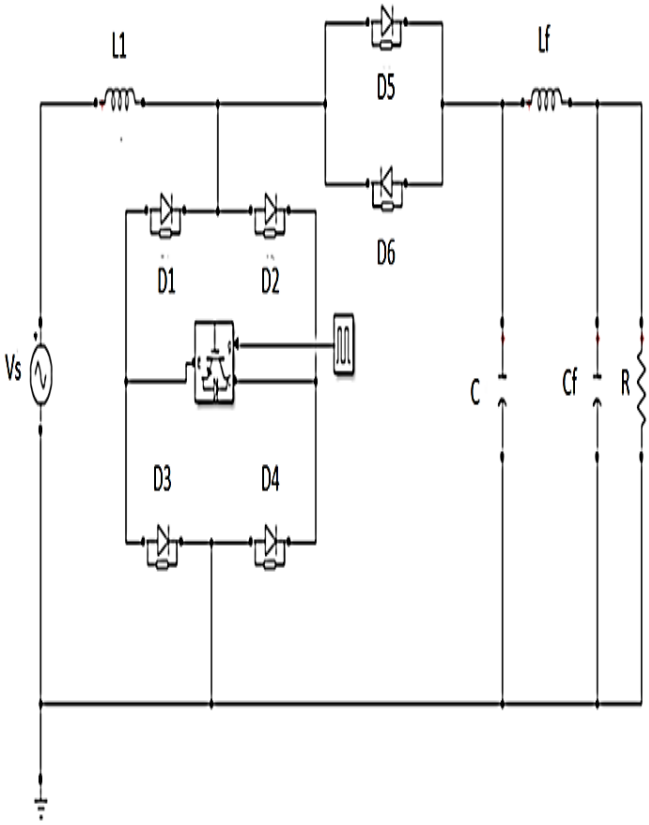
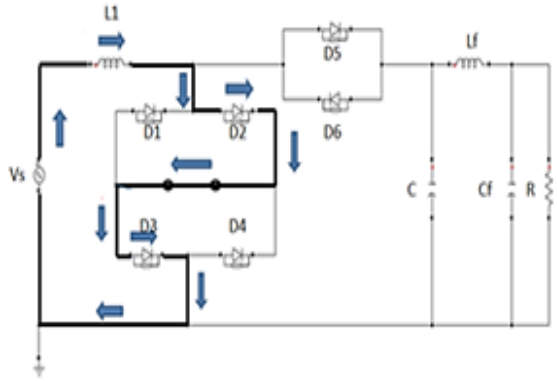


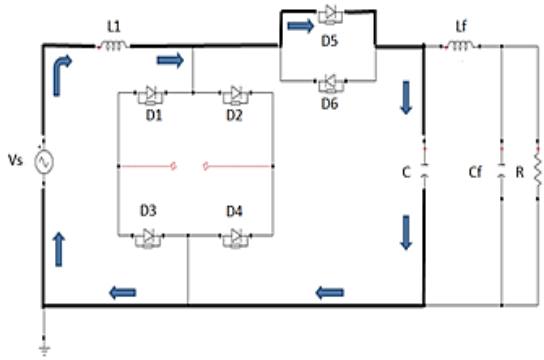
Fig. 1: The modified AC-AC boost converter.

is needed to compensate the missing voltage during the sag. This topology is working as a boost circuit, and the voltage will be controlled by a new control method on the duty-cycle of the switch to obtain the desired value of load voltage. The LC low-pass filter (L_f, C_f) is used to provide a pure sinusoidal voltage at the load. The values of L_f and C_f are selected according to the following criterion:

$$Signal\ freq. < \frac{1}{2\pi\sqrt{L_f C_f}} < Switching\ freq.$$



(a)



(b)

Fig. 2: The operating mode during the positive half cycle when the transistor is (a) switched ON and (b) switched OFF.

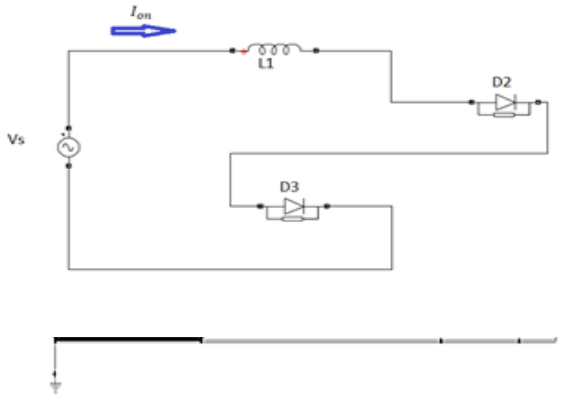
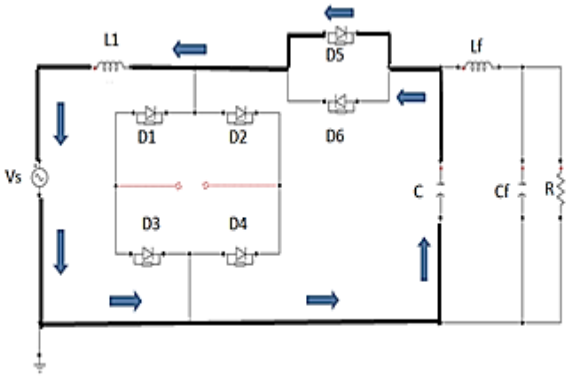


Fig. 4 Simplified circuit model when the switch is ON.

(a)



(b)

Fig. 3: The operating mode during the negative half cycle when the transistor is (a) switched ON and (b) switched.

b. Modeling and Analysis

From the operating principles in both positive and negative half cycles, we observe that both of them are the same, so the model will just be studied for the positive half cycle as follow:

(a) When the switch is ON :

The simplified circuit is shown in Fig. 4 when the switch is ON.

$$V_{L1} = V_S \qquad (1)$$

$$L_1 \frac{\mathrm{d}\, I_{ON}}{\mathrm{dt}} = V_S \qquad (2)$$

$$I_{ON} = \frac{1}{L_1} \int V_S \,\mathrm{dt} \qquad (3)$$

Where:

V_{L1}: inductor voltage.

V_S : supply voltage.

I_{ON}: the current at switch ON.

(b) When switch is OFF :

The simplified circuit is illustrated in Fig. 5.

$$V_{L1} = V_S - V_C \qquad (4)$$

$$L_1 \frac{\mathrm{d}I_{OFF}}{\mathrm{dt}} = V_S - V_C \qquad (5)$$

$$I_{OFF} = \frac{1}{L_1} \int (V_S - V_C)\mathrm{dt} \qquad (6)$$

Where:

V_C: capacitor voltage.

I_{OFF}:the current at switch OFF.

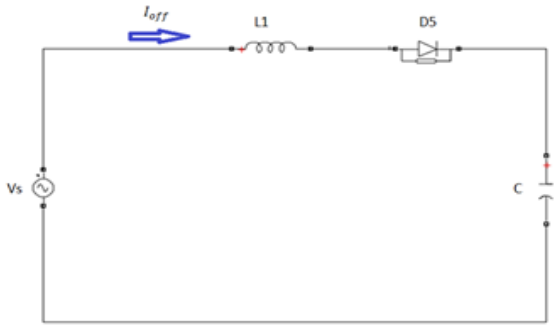


Fig. 5 Simplified circuit model when the switch is OFF.

The energy required to maintain the load-voltage during one half cycle can be derived as follows:
It's known that:
Energy =Time * Power

$$P_{ref} = V_{ref} * I_{ref} * \cos\phi = P_o \quad (7)$$

where: Po is the rated load power.
When the sag occurs, the missing power (Pmiss) is expressed as:

$$P_{miss} = (V_{ref} - V_{sag}) * I_{ref} * \cos\phi \quad (8)$$

$$\frac{P_{miss}}{Po} = \frac{((V_{ref} - V_{sag}) * I_{ref} * \cos\phi}{V_{ref} * I_{ref} * \cos\phi} \quad (9)$$

$$P_{miss} = \frac{(V_{ref} - V_{sag})}{V_{ref}} P_o \quad (10)$$

$(V_{ref} - V_{sag}) = \Delta V$ = r.m.s. value of missing voltage (11)

$$P_{miss} = \frac{\Delta V}{V_{ref}} P_o \quad (12)$$

Then the energy will be:

$$E = \frac{T_o \Delta V}{V_{ref}} P_o \quad (13)$$

where:
V_{ref}: rated value of the load voltage.
T_o: the supply voltage time
For half cycle of operating:

$$E_o = \frac{T_o \Delta V}{2 V_{ref}} P_o \quad (14)$$

III. PROPOSED CONTROLLER

To maintain the load voltage at its rated voltage, a special control strategy must be adopted to control the duty-cycle of the switch which determines the boost converter output voltage. There are many control strategies used to obtain the suitable value of the duty-cycle such as PI controller method, discrete state space control method, self-tuned fuzzy control method, and neural network controller as in [13-20].

In this paper, a new control method is adopted by obtaining a mathematical relation between the duty-cycle and the voltage gain of the proposed topology (where the voltage gain represents the ratio of the output rated load voltage to the supply voltage). The solid line of Fig. 6 demonstrates the simulated voltage gain for different duty cycle values. Almost a linear relationship between the duty-cycle and the boost circuit voltage gain is observed. As a result, a linear interpolation can provide an accurate estimation for this relationship. After performing the suitable steps of interpolation, the following equation is found to be a very good approximation for the simulated values of the gain (see the dotted line in Fig. 6). The characteristics given in Fig. 6 are valid for all load values greater than or equal to 50 Ω.

By taking any two points on the straight line of Fig. 6, for example (1, 0.54) and (3.5, 0.04), then applying the equation of the straight line, the resulted formula connecting duty cycle with the gain will be as follows:

$$D = -0.205G + 0.7505 \quad (15)$$

$$G = V_{ref}/V_S \quad (16)$$

where:
D: Switching duty-cycle.
G: Voltage gain.
Fig. 7, illustrates the complete proposed boost converter circuit with the controller. In the control circuit, the supplied voltage is converted into a DC voltage proportional to its r.m.s value ($V_{in,DC}$). According to the conversions happened in the control circuit, the voltage gain can be re-written in term of the input $V_{in,DC}$ and the

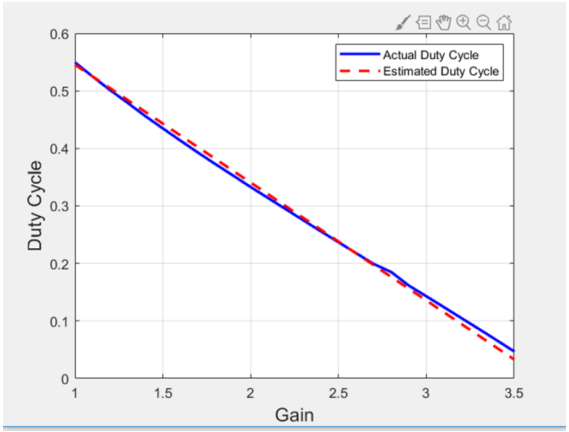


Fig. 6 The relationship between the Duty-cycle and voltage gain of the proposed.

equivalent DC reference voltage ($V_{ref,DC}$) as follows:

$$G = V_{ref,DC}/V_{in,DC} \qquad (17)$$

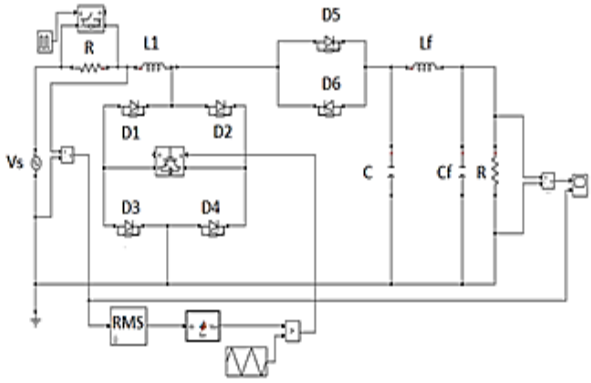


Fig. 7 Proposed topology with control circuit.

The trigger signal of the transistor is obtained from the pulse width modulation (PWM) circuit.
The signal entering the PWM is compared with a symmetric triangular wave with amplitude range [-1, 1]. By studying the resulted PWM duty cycle with respect to the value of the DC input PWM voltage (V_{PWM}), an equation can be evaluated to perfectly express the relationship between V_{PWM} and the duty cycle of the PWM as follows:
When V_{PWM} is equal to the upper limit of triangular wave, duty-cycle will be equal to 1. However, the duty cycle is equal to 0 when V_{PWM} is equal to the lower limit of the triangular wave.
Due to the linearity behavior of the triangular wave, the equation connecting the duty cycle with V_{PWM} can be expressed by a straight line. The same as equation (15), by taking two points on the straight line of Fig. 8 which represents the relationship between the duty cycle and V_{PWM}, such as (-1,0) and (1,1), the required formula can be expressed as follows:

$$V_{PWM} = 2D - 1 \qquad (18)$$

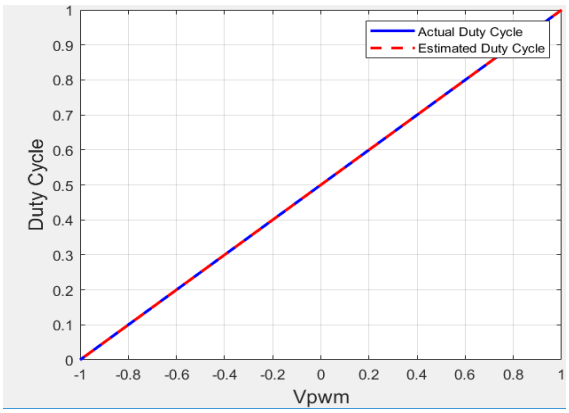


Fig. 8 The relationship between the Duty-cycle and PWM voltage.

The proposed control circuit with the indicated voltages is shown in Fig. 9.

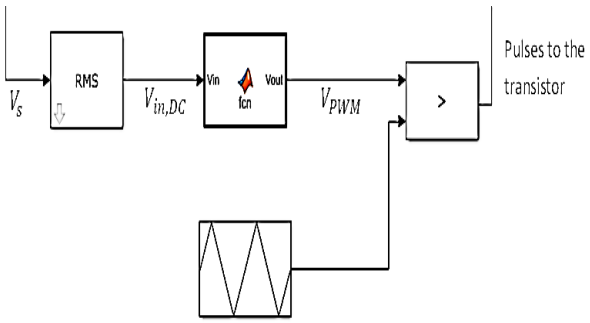


Fig. 9: Proposed control circuit.

Any reduction in the supply voltage Vs during the sag leads to change $V_{in,DC}$. This means that the boost converter needs to produce the gain value given in Equation (17) to compensate the missing value of voltage. The following steps demonstrate the proposed control algorithm of compensating the voltage sag:

- From Equation (17) the voltage gain is calculated.

- Form Equation (15), the suitable duty cycle that compensate the voltage sag is calculated.
- The required input voltage to the PWM that generates the intended duty cycle is calculated from Equation (18).

The above algorithm is implemented using MATLAB block user define function (fcn) shown in Fig. 9

IV .SIMULATION RESULTS

Fig. 10 shows the simulation results of the proposed topology with two levels voltage sag, with system parameters as in Table (1). The voltage drops from 311 peak voltage to 150 volt at

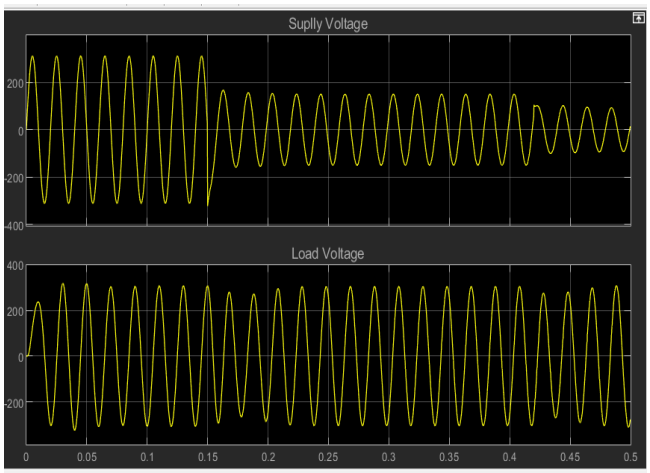


Fig. 10 the simulation result of the supply and load voltage at sag.

Table (1) The modified system parameters.

0.15 sec., then falls to 94 volt at 0.41 sec.

parameter	value
Nominal voltage	220 volt r.m.s
Line frequency	50 Hz
Switching frequency	8kHz
Capacitor C	20μF
Inductor L1	5mH
Filter inductor	10mH
Filter capacitor	600μF
Load	100Ω

The first sag reduces the voltage to 48% of its reference level (sag depth 52%), while the second sag reduces the voltage to 30% of the reference voltage (sag depth 70%). It is clear from Fig. 10 that the proposed circuit effectively compensates the voltage sag in spite of the noticeable reduction in the supplied voltage. In addition, the response of the proposed circuit is independent of the load variation, and it is very cost effective since it requires only single switch in its operation.

V. CONCLUSION

This paper has presented a proposed topology for voltage sag mitigation with new control strategy. With the aid of a modified single switch boost converter, voltage sag depth up to 70% has successfully been compensated. Since the proposed circuit uses a single switch transistor, it is very cost effective with low complexity of operation. The new control method proposed in this work depends on presenting a mathematical model between the duty-cycle and the voltage gain of an AC-AC boost converter, and another model connecting the input voltage of the PWM circuit and the resulted duty cycle. The operating principles and modeling equations are explained in detail by circuit analysis. The simulation results accentuate the effectiveness of the proposed topology in compensating the missing voltage of deep and long duration voltage sag. In addition, the results exhibits the pure output sinusoidal voltage resulted from attaching the LC low-pass filter to the boost converter output.

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