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Original Article

Analog Programmable Circuit Implementation for Memristor

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Abstract: *In this work, a new flux controlled memristor circuit is presented. It provides a tool to emulate the pinched hysteresis loop. When driven the memristor by a bipolar periodic signal, the memristor exhibits a "pinched hysteresis loop" in the voltage-current plane and starting from some critical frequency, the hysteresis lobe area decreases monotonically as the excitation frequency increases, the pinched hysteresis loop shrinks to a single-valued function when the frequency tends to infinity. The design model numerically simulated and the physical implementation is achieved by using a field programmable analog array (FPAA). The circuit can be modeled and implemented with a changeable nonlinear function blocks and fixed main system blocks. The simplicity of the specific design method makes this proposed model be a very engaging option for the design of the memristor.*

***Index Terms*— Field programmable analog array (FPAA), Memristor, Circuit emulator, Pinch hysteresis loop.**

I. INTRODUCTION

As the fourth passive component, a memristor is the two-terminal passive component with a unique non-linear feature, which is not observed in other two-terminal components like inductors, resistor or capacitors. Even though the behavior of memristor was investigated two centuries ago [1], implementing a memristor was hypothetically proposed by L. Chua in 1971 for the first time [2]. Chua and Kang broadened this thought by clarifying the major properties of memristive devices in 1976 [3]. Afterward, in 2008, S. Williams and his group from the HP lab was the first gathering to create the material structure of a memristor using T_iO_2, but until then it was only a theoretical concept [4]. The memristor is the only nanoscale device that can show the missing link between electrical charge and magnetic flux. In the current-voltage plane, it shows a unique hysteresis loop pinched at the origin. It is a special type of resistor, where the resistance increases/decreases depending on the polarity of either the current passing through it or the applied voltage. The removal/zero value of the excitation source doesn't change the memristor resistance (memristance). This property gives the memristor the capability to act like a memory. Since the introduction of the HP memristor model, many engineers and scientists have shown a huge interest to understand and investigate the potential applications of this two-terminal non-linear and nanoscale device. Many papers have been appeared in literatures to explore the possibility of utilizing this gadget in different applications like high speed memory arrays using neuromorphic circuits, neural networks, analog and digital circuits, adaptive filters and sinusoidal and relaxation oscillators [5-6]. Inserting the

memristor in the system can simply generates a chaotic signal, which improves research interests in the design of the chaotic memristive circuits, because of the nonlinearity of memristor device [7]. Itoh and Chua [7] replacing Chua's diodes with memristors described by monotone -increasing and piecewise-linear function, and derived several oscillators from Chua's oscillators. Pham et al. proposed a memristor model and insert it in system with hidden attractors [8]. The first memristor emulator proposed by L. Chua, based on active devices [2]. However, this emulator circuit is relatively complex and huge. Recently, grounded memristor emulator circuits built with analog multipliers and op-amps have been proposed in [9, 10]. Muthuswamy [11] proposed a flux-controlled memristor with a cubic characteristic based on a relatively simple analog circuit. It comprises two op-amps and two multipliers and analog integrator. Yu et al. [12] Proposed a flux-controlled memristor emulator with floating terminals by making use of one op-amp, four current conveyors, one capacitor, one multiplier, and several resistors. This memristor emulator has the ability of being utilized both in floating connections and grounded connections. H. Kim [13], proposed a memristor which is involve of an adder, eight resistors, ten transistors and five op-amps another emulator has been introduced in [14], which requires five Differential Difference Current Conveyors (DDCC), four CMOS blocks, one capacitor and four resistors. Some emulators are appropriate for computer based simulation, but not for testing as hardware, whereas some are not fit for integration in a complex circuit [15] [16]. Pershin and Ventra were proposed a memristor emulator [17] using digital and analog mixed circuits. M. Fouda, Z. Khalifa, [18] were proposed emulator memristor circuit consist of one multiplier and two current conveyers.

FPAA (Field Programmable Analog Array) is a programmable gadget for executing a rich assortment of systems including analog functions. Since this electronic gadget has a characteristic that can be utilized to change component values and interconnections programmatically, it can be dynamically reconfigured. This implied that a design modification or a totally new design can be executed with reconfigurable FPAA gadget. In this procedure, there is no need to reset or to power down the system. In addition, FPAA gives more efficient and economical solutions for dynamical system designs. Utilizing FPAAs, different dynamical systems, including different complex systems can be executed easily at low cost, in a substantially with increased reliability and component stability [19–20]. In this work, for the first time the memristor proposed model has been realized by FPAA.

The paper is organized as follows: Sec. II, shows the memristor properties and the characteristics of the pinch hysteresis loop. Sec. III, the proposed a new memristor model and the pinch hysteresis loops are proposed and numerically simulated. Programmable Circuit implementation using the FPAA will be introduced in Sec. IV. A Conclusions are finally drawn in Sec. V.

II. MEMRISTOR CHARACTERSTICS

When the device has three significant fingerprints, Adhikari et al. [21]. Accordingly, it can be considered as a memristor, any memristor emulator circuit should likewise agree to these three fingerprints or defining properties:

Memristor Fingerprint 1: The first significant signature of the memristor is Pinched Hysteresis Loop, its unique pinched hysteresis loop which recognize it from any device that is not memristive in the (current-voltage) plane.

(a) The Lissajous figure of all memristors, having positive memristance and operated by a sinusoidal signal of any frequency and amplitude, have to go through the origin, In (current-voltage) plane.

(b) The amount of memristor's voltage and current in the Lissajous figure ought to be same only when it will pass through the origin, for whatever is left of the time (current-voltage) ought to have different values.

Memristor Fingerprint 2: Hysteresis loop area increases as frequency decrease. The second characteristic of the memristor is the inversely proportional relationship between the memristors hysteresis lobe area and frequency of periodic operating signal; with the increment of frequency, the lobe area will decrease.

Memristor Fingerprint 3: At an infinite frequency, there are no loops. At a very high frequency, the memristors will behave as a linear device like a resistor, so memristor loses its unique non-linearity and the amount of voltage and current stay the same for all times in the $(\text{current} - \text{voltage})$ plane.

A portion of the intriguing memristor properties are:

• The memristor does not storage energy.

• A memristors system can also be described as a single memristor, Similar to classical circuit elements.

• Non-linear relationship between memristor's current and voltage.

• By the memristor, Memory capacities based on different resistances are produced.

• If the magnetic flux and electrical charge through the memristor have a positive relationship (memristance greater than zero), non-volatile memory is possible.

III. THE PROPOSED MODEL

The concept of memristor as the fourth circuit element was proposed by L. Chua in 1971 [2]. It shows the relationship between two fundamental circuit variables, the flux $(\emptyset)$ and the charge (q). Hence, there are two types of memristor: flux-controlled and charge-controlled memristor [2]. A charge-controlled memristor is depicted by:

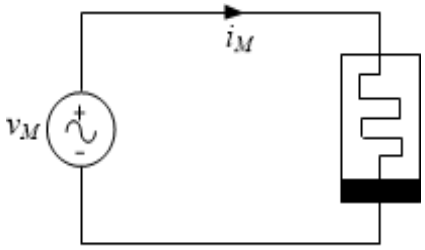


Fig. 1 Memristor symbol

$$v_M = M(q) i_M \tag{1}$$

where v_M and i_M are the voltage across the memristor and the current through the memristor, respectively.

Here the memristance $M(q)$ is described by

$$M(q) = \frac{d\emptyset(q)}{dq} \tag{2}$$

while the flux-controlled memristor is given by

$$i_M = W(\emptyset) v_M \tag{3}$$

where $W(\emptyset)$ is the memductance, which is described by:

$$W(\emptyset) = \frac{dq(\emptyset)}{d\emptyset} \tag{4}$$

This work considers the flux–controlled memristive system, as shown in Fig. 1. The circuit equations described by [3]:

$$\begin{cases} \dot{x} = F\,(x\,, u\,, t) \\ y = G\,(x\,, u\,, t)\,u \end{cases} \tag{5}$$

Where u, y, and x denote the input, output and state of the memristive system, respectively. The function F is a continuously differentiable, n-dimensional vector field and G is a continuous scalar function.

Based on the definition of memristor (5), a proposed new memristive model by using the trigonometric function tan inverse is given as:

$$\begin{cases} h(x_1, x_2) = (bx_2 - tan^{-1}(x_2))x_1 \\ \dot{x}_2 = ax_1 \end{cases} \tag{6}$$

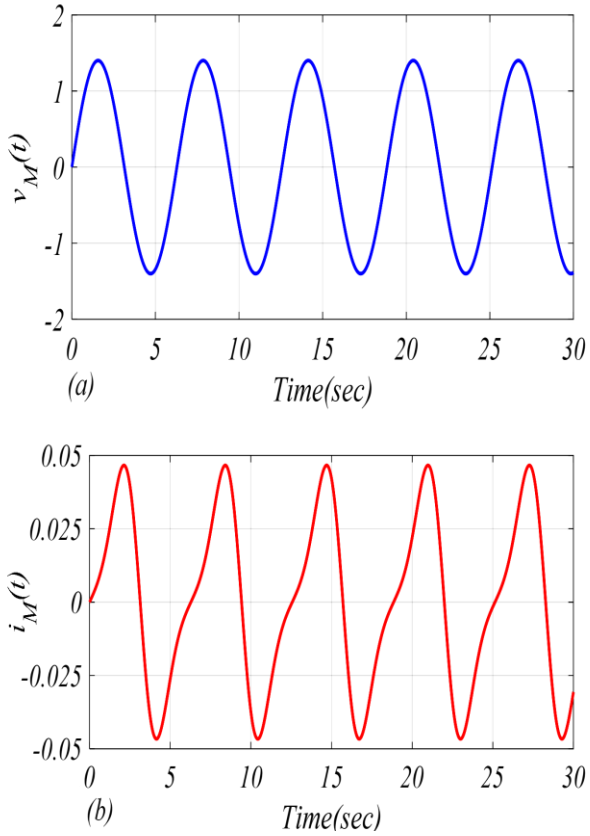


Fig. 2 (a) input voltage waveform, $A = 1.4V$ and $\omega = 1$ rad/sec, (b) memristor current waveform $\omega = 1$ red/sec.

where x_1 and x_2 are the input and internal state of the memristor. Here $h(x_1, x_2)$ represents the output of the memristor while a and b are positive parameters.

The memristor constituent relation, is described analytically by the following equation:

$$q = \frac{\emptyset^2}{4} - \left(\emptyset \tan^{-1}(\emptyset) - \frac{1}{2}\ln(1+\emptyset^2)\right) \qquad (7)$$

By applying sinusoidal voltage source as shown in Fig. 2 (a) and defined by:

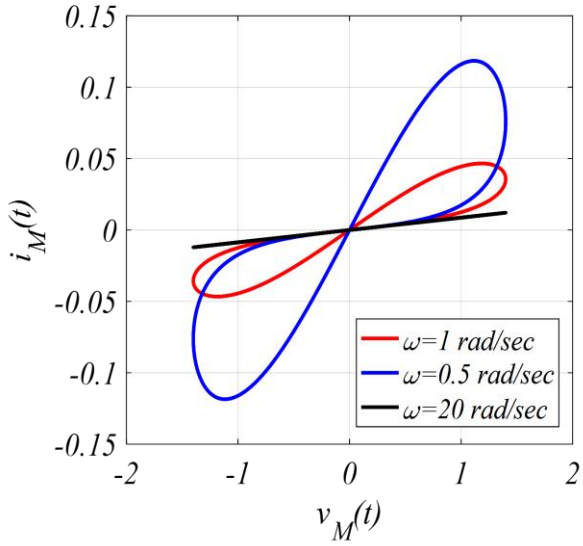


Fig. 3 Pinch hysteresis loop of the proposed memristive model (6) driven by a sinusoidal stimulus, when $A = 1.4V$, $x_2(0) = 0.3$ and varying frequency.

$$\begin{cases} v_M = A\sin(\omega t) & t \geq 0 \\ 0 & t < 0 \end{cases} \qquad (8)$$

across the memristor, with $A = 1.4V$ and $\omega = 1rad/s$. The current response $i_M(t)$, as shown in Fig. 2 (b) and charge $q(t)$ equations as in (9) and (10) respectively, at the bottom of page.

When the parameters are set to: $a = 2, b = 0.5$ and $x_2(0) = 0.3$, the voltage–current relationship of the flux-controlled memristor, for sinusoidal inputs for different values of ω, is depicted in Fig. 3, which prove the hysteresis loop characteristics of the memristor [21]. When the frequency of the wave input is very high, the pinched hysteresis loop shrinks to a single-valued function as shown in Fig. 3 at $\omega = 20rad/s$.

$$i_M(t) = \left[\frac{A}{2\omega}(1-\cos(\omega t)) - \tan^{-1}\left(\frac{A}{\omega}(1-\cos(\omega t))\right)\right] A\sin(\omega t) \qquad (9)$$

$$q(t) = -\left[\frac{A}{\omega}(1-\cos(\omega t))\tan^{-1}\left(\frac{A}{\omega}(1-\cos(\omega t))\right) - \frac{1}{2}\ln\left(1+\frac{A^2}{\omega^2}(1-\cos(\omega t))^2\right)\right]$$

$$+\frac{A^2}{4\omega^2}(1-\cos(\omega t))^2 \qquad (10)$$

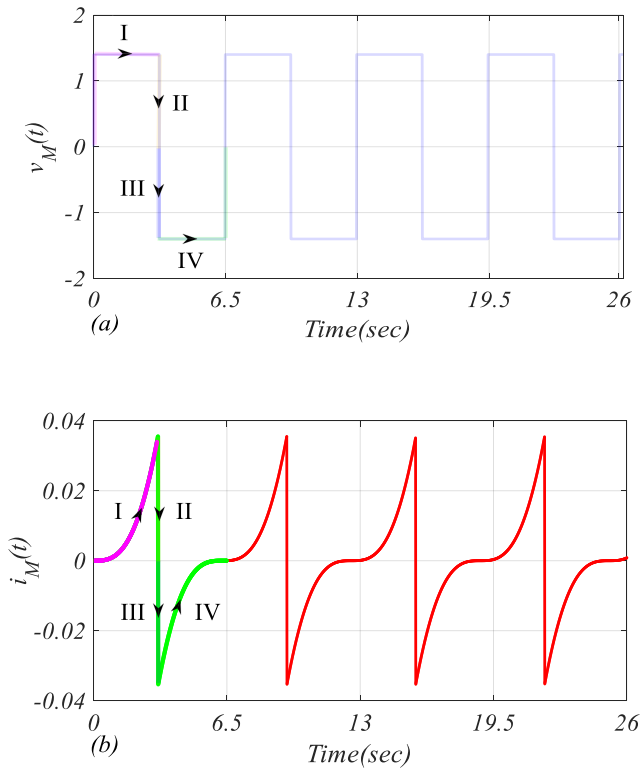


Fig. 4. The memristor square wave excitation, response and characteristic regions: (a) input voltage square wave ($A = 1.4V, \omega = 1rad/s$), (b) memristor current.

By applying the square wave input voltage for memristor as shown in Fig. 4 (a), and defined by:

$$v_M = \frac{4A}{\pi}\sum_n^{\infty}\frac{1}{n}\sin(0.3\pi nt) \qquad (11)$$

Where $A = 1.4V$ and $n = 1,3,5,\cdots$

across the input of memristor model (6). The current response $i_M(t)$, as illustrated Fig. 4 (b), and charge $q(t)$ equations shown in (12) and (13) respectively at the bottom of the page.

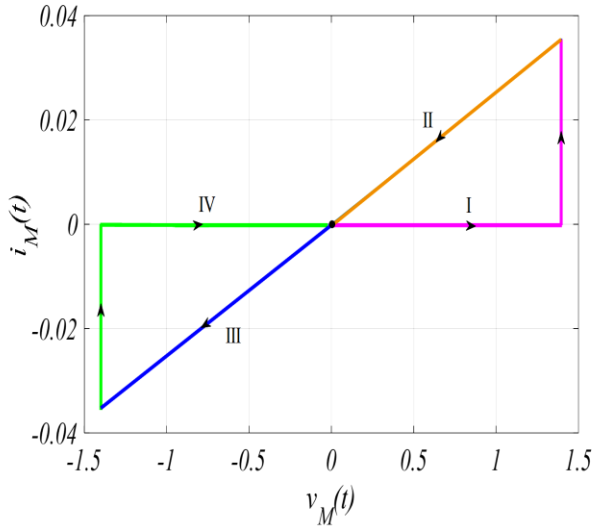


Fig. 5 Pinch hysteresis loop of the proposed memristive model (6) driven by a square wave, $A = 1.4V$, $x_2(0) = -1$ and frequency $\omega = 1\,rad/s$.

When $a = 2$, $b = 0.5$ and initial condition $x_2(0) = -1$, the voltage–current relationship of the flux- controlled memristor, for square wave input with $\omega = 1rad/s$, plotted in Fig. 5, which prove the hysteresis loop characteristics of the memristor [21].

When the memristor input voltage $v_M(t)$ is a square wave, the curve obviously demonstrates the memory effect. It is seen from the graph of both $v_M(t)$ and $i_M(t)$ in Fig. 5. In the interval when $v_M(t)$ is constant, the flux $\emptyset(t)$ follows a linearly decreasing or increasing course, which results in a similar effect on the memductance $W(t)$ and consequently also on the current $i_M(t)$. As soon as the constant input voltage becomes zero, $v_M(t) = 0$, the memductance stays constant until the next change in $v_M(t)$. The Current $i_M(t)$, then abruptly change and the range of this change depends on the final $W(t)$ value 'remembered' by the memristor.

$$i_M(t) = \left[\frac{2.1A}{\pi}\sum_n^{\infty}\frac{(1-\cos(0.3\pi nt))}{n^2} - tan^{-1}\left(\frac{2.1A}{\pi}\sum_n^{\infty}\frac{(1-\cos(0.3\pi nt))}{n^2}\right)\right]\frac{4A}{\pi}\sum_n^{\infty}\frac{\sin(0.3\pi nt)}{n} \qquad (12)$$

$$q(t) = \frac{4.5A^2}{\pi^2}\sum_n^{\infty}\frac{(1-\cos(0.3\pi nt))^2}{n^2} - \left[\frac{2.1A}{\pi}\sum_n^{\infty}\frac{(1-\cos(0.3\pi nt))}{n^2}tan^{-1}\left(\frac{2.1A}{\pi}\sum_n^{\infty}\frac{(1-\cos(0.3\pi nt))}{n^2}\right)\right.$$
$$\left. -0.5\ln(1+\frac{18A^2}{\pi^2}\sum_{n5}^{\infty}\frac{(1-\cos(0.3\pi nt))^2}{n^2})\right] \qquad (13)$$

IV.FPAA IMPLEMENTATION OF MEMRISTOR MODEL

The FPAA used, AN221E04, is mounted on the development board AN221K04 from Anadigm [22]. The architecture of AN221E04 is shown in Fig. 6. AN221E04 comprises a $2x2$ matrix of configurable analog blocks (CABs). Configuration data is stocked in an on-chip SRAM configuration memory. The four CABs have access to single Look Up Table (LUT), with the capacity 256 Byte, which displays a new method of checking any programmable element within the gadget in response to a signal or time base. It can be used to execute arbitrary input-output transfer functions. Analog input signals can be connected with the outside world via the four Input/output cells. Output signals can be routed from within the array out through Input/output Cells directly. The FPAA can be accepted either generate its own clock using an on-chip oscillator and an external crystal or an external clock.

FPAA is depends on switched capacitor (SC) technology. Switched capacitor circuits are acknowledged with the utilization of some fundamental building blocks, such as switches, capacitors, op-amps and non-overlapping clocks. The operation of these circuits is depending on the standard of the resistor equivalence of a switched capacitor.

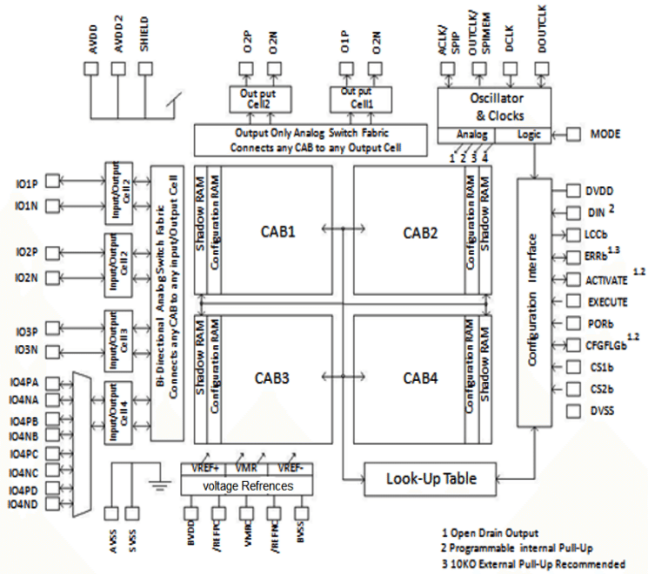


Fig. 6 Architecture of the AN231E04 FPAA.

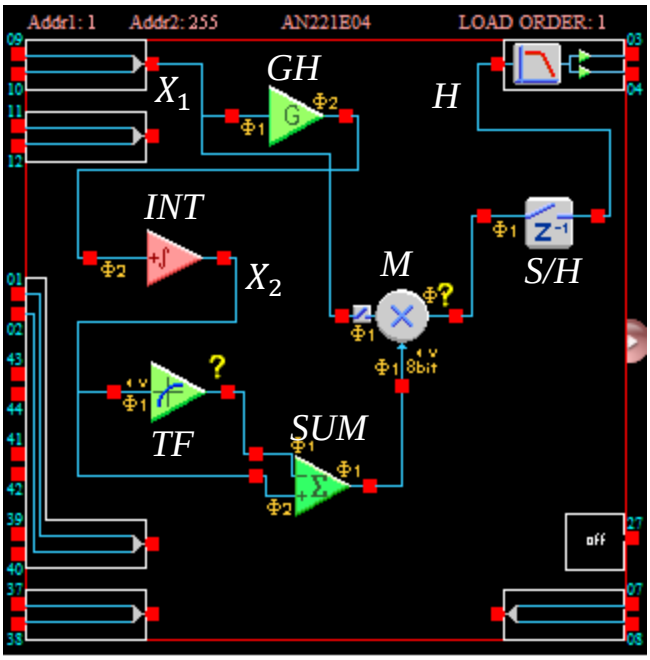


Fig. 7 Circuit scheme of memristor model by FPAA.

The model is downloaded to the FPAA chip on the development board by means of serial interface, After modelling system implemented in an FPAA software tool.

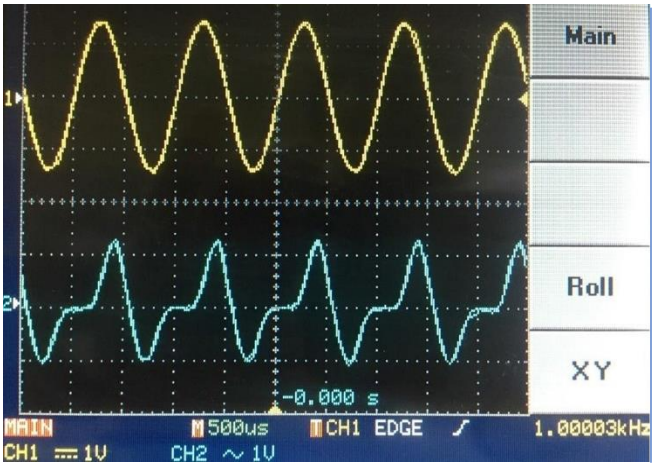
The proposed memristor model (6) is implemented by FPAA as follows:

$$\begin{cases} H(X_1, X_2) = (bX_2 - tan^{-1}(X_2))X_1 \\ \dot{X}_2 = aX_1 \end{cases} \quad (14)$$

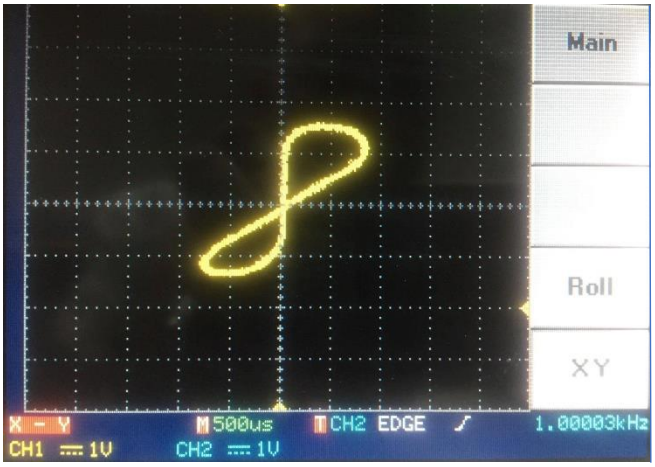
All circuit parameters are programmable and their values cannot be exactly fixed. They are executed with some parameter tolerances. Moreover, introducing further parameters in the system (14) was necessary in order to control the inaccuracies due to the programmable device, so the model executed on the FPAA, can be written as follows:

$$\begin{cases} H(X_1, X_2) = G_1(bX_2 - tan^{-1}(X_2))X_1 \\ \dot{X}_2 = aG_2X_1 \end{cases} \quad (15)$$

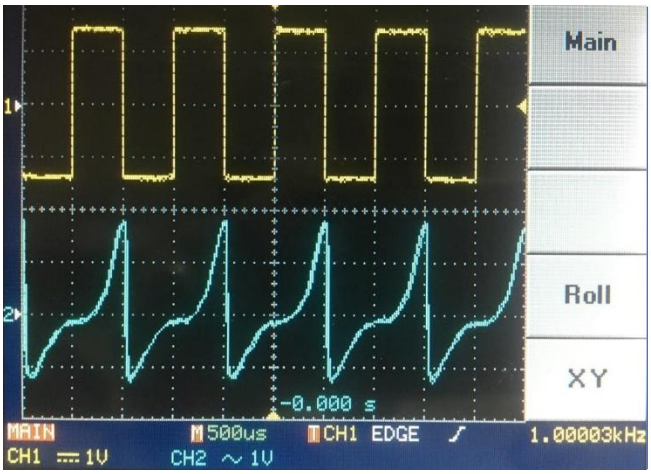
The parameters $G_i(i = 1,2)$ are experimentally tuned to control by these inaccuracies. The circuit scheme is shown in Fig.7. The main block useful to implement *a tan inverse function* is a user-defined function (Transfer Function-LUT) CAM.



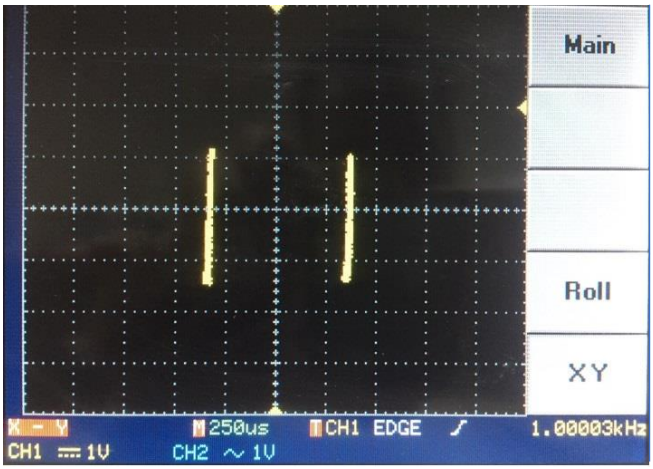
(a)



(b)



(c)



(d)

Fig. 8 Experimental results. The oscilloscope observations, time series trends and corresponding phase portrait of the input voltage $v_M(t)$ and memristor current $i_M(t)$;(a) and (b) for sinusoidal wave input, (c) and (d) for square wave input.

This CAM executes a user-specified voltage transfer function with 256 quantization steps. It creates a specified output voltage in response to the value of the sampled input voltage. The Successive Approximation Register (SAR) and Look Up Table (LUT) used to perform Analog to Digital Converter (ADC) on the input and generate the appropriate user-defined output voltage. The FPAA device comprise a single 256 byte LUT [23].

The integration constant for integrator(INT) is set to $0.09\ 1/\mu s$. User defined function (TF) in the scheme is used to implement the *tan* inverse function. *GH* multiplies X_1 by a constant value equal to 0.1 and the output of the *GH* is an input to the integrator *INT* part. The block *SUM* sums the two terms (*tan* inverse function and X_2). The multiplier block *M* used to multiply (X_1 *by* the result of *SUM*), *S/H* is sample and hold block, *H* is the output of the memristor model.

A reconstruction filter was selected at the OutputCell1 to remove the higher frequency components that are introduced by sampling action of the SC CAMs. The filter corner frequency (76-470 kHz) should be set based on the signal frequency and the sample clock rate. This filter parameter should be far enough above the highest frequency component of the signal so that the

signal is not attenuated and far enough below the sampling frequency set by the sampling clocks so that the higher frequency components are attenuated.

The CAMs are designed to use one clock A, except the multiplier CAM is designed to use two clocks (clock A and clock B). The frequency of clock B should be set at 16 times the frequency of clock A. Clock A is the clock driving the switched capacitor portion of this CAM. All switched capacitor clocks within a single signal path should typically use the same clock frequency. Clock B is the clock driving the successive approximation register (SAR). The faster SAR clock is required for correct operation of this circuit. When clock B=1600 kHz; the clock A=102 kHz.

The experimental characteristics of the implemented memristor model were observed using digital oscilloscope. Fig. 8 (a) and (b) shows the time evolution of sinusoidal input and output of the memristor and the hysteresis loop which driven by sinusoidal Input. Fig.8(c) shows the time evolution of square wave input and output of the memristor and (d) shows the pinch hysteresis loop which driven by square wave input. Channel 1 display the signal taken from function generators, while Channel 2 displays the signal taken from OutputCell1 pins of FPAA.

V-Conclusion

This paper, introduced a new memristor emulator circuit. The design and realization of the memristor circuit depend on an analog programmable device, FPAA, which gives the possibility of experimentally exploring the various dynamics of the memristor circuit in a rapid and low-cost way.

The circuit dynamics are investigated experimentally under various sets of parameter values. The monitoring results explain very good agreement between numerical simulation and experiment. This is a stimulus, for the future, to extend practical researches and demonstrations over to other types of circuits.

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