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Matlab/Simulink Modeling of Parallel Resonant DC Link Soft-Switching Four-leg SVPWM Inverter

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Abstract: *This paper suggests the use of the traditional parallel resonant dc link (PRDCL) circuit to give soft switching to the Four-leg Space Vector Pulse Width Modulation (SVPWM) inverter. The proposed circuit provides a short period of zero voltage across the inverter during the zero-vectors occurrence. The transition between the zero and active vectors accomplished with zero- voltage condition (ZVC), this reduces the switching losses. Moreover, the inverter output voltage Total Harmonic Distortion (THD) not affected by circuit operation, since the zero voltage periods occur simultaneously with zero-vector periods. To confirm the results, balanced and unbalanced loads are used. Matlab/Simulink model implemented for simulation.*

***Index Terms*—Four-leg SVPWM inverter, Parallel resonant DC-Link inverter, Total Harmonic Distortion, Zero-voltage switching.**

I. INTRODUCTION

In power electronics pulse-width-modulation converters when the switches work, the load current turned ON or OFF during each switching action, therefore these switches subjected to high stress and high power losses, which increases with the switching frequency of the PWM. The other disadvantage of the switching operation is the electromagnetic interference EMI that results from the large and rapid rise of the voltage and current. These effects of switching increase linearly with respect to the switching frequency. Switching losses have an impact on the converter size, weight, and power capability. Therefore, by reducing these losses, switching at high frequencies is applicable. This can be achieved if the converter switches changes its state (from ON to OFF or vice versa) when the current through or voltage across these switches is zero at the time of switching. The increased demand for high power converters in aerospace, military, and telecommunication applications required the design of converters that can work at high switching frequency with less effect of switching losses. These applications have other constraints regarding weight, size, and temperature of the converters to handle greater loads. To overcome these problems, applying soft switching is essential[1-6]. The advantages of high frequency converters have recognized, moreover, their importance has much increased.

High switching frequencies used to reduce the sizes of passive components. Tradeoffs between switch ratings and converter size should make, but it is hard to find a good solution for high-voltage, high-step-down ratio, and low-power applications[7]. Marked efforts have made in development of high-frequency Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) dc-ac power converters, which can now recognize converters that operate with high performance, and negligible noise. The principle of resonance used with these converters in order

to make the soft-switching techniques (ZVS/ZCS) in the resonant link and the device. For inverters these resonant links placed in different locations depending upon their configuration. The soft switching techniques saw a great progress through various stages during the last two decades.

II. Parallel Resonant DC Link (PRDCL) Four-leg Inverter

The first (PRDCL) circuit presented in[8], where the authors claimed that it is capable of providing high-frequency, three-phase dc-ac power conversion. Figure 1 shows the proposed circuit of a parallel resonant DC link with four-leg inverter.

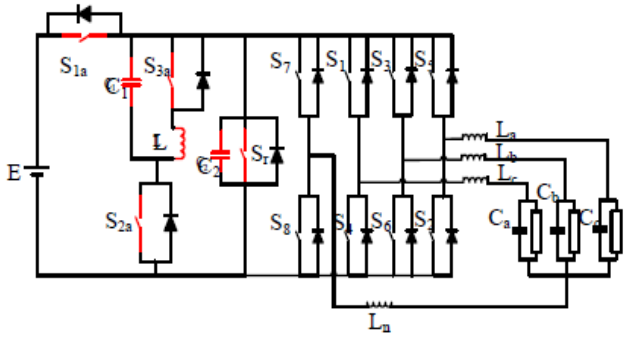


Fig.1 PRDCL circuit with four-leg inverter.

To accomplish zero voltage switching a PRDCL with four-leg inverter system is proposed as shown in Fig.1, where the four-leg inverter operates as a Space Vector PWM inverter. A PRDCL circuit is added between the dc source and the inverter, to decrease the switching losses in the system, the circuit shown in Fig.1, forces the DC link voltage across the inverter to become zero for a short duration, at each time the zero voltage space vector (1111) or (0000) appears in the switching sequence cycle. As a result, PRDCL circuit minimizes the switching losses of the inverter system since at each switching cycle the resonance circuit operates twice making the status change of the switches in the inverter at that instant of time to be turn-on or turn-off at zero voltage across them.

III. Simplified Circuit Model

As shown in Fig.1, a PRDCL circuit composed of L, C1, and C2 placed between the dc voltage source E and the four-leg SVPWM inverter. Three controllable switching devices used in the circuit topology. The switch (Sr) is redundant, since it is in parallel with the inverter, where both switches in any inverter leg can turn on at the same time to do its function. The operating function of these switches is explained in various operation modes in the next section. In Fig.1 the inverter filter inductance (Lac) is greater than the resonant circuit inductance (L)[8, 9]. The inverter system in Fig.1 can simplified to for each resonant cycle as shown in Fig.2. However, the value of the current source Io that represents the input current to the inverter in the period of each resonant cycle, depends on the individual load phase currents and the states of the eight-inverter devices. For a given SVPWM, Io (magnitude and direction) could be very different during switching cycles.

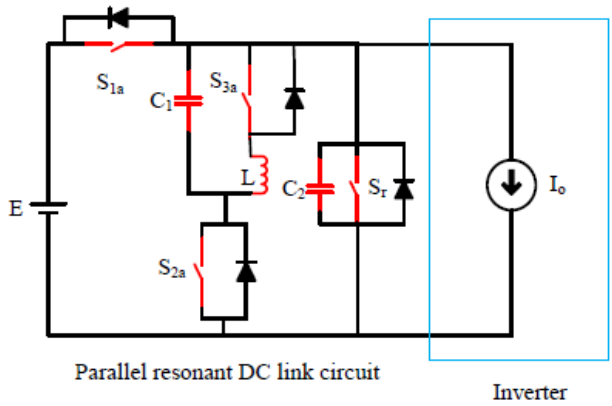


Fig.2 Simplified circuit diagram for duration of each resonant cycle.

IV. Circuit Operation Modes

The circuit analysis and operation for a three-leg inverter are discussed in detail in [8] and [9]. The same analysis is considered in the work for four-leg inverter. Figure 3 shows the resonant operating modes.

Mode-1 [t_o-t_1] At t=t_o it assumed that the zero voltage vector acts according to the SVPWM sequence strategy, i.e. the upper switches (S_1, S_3, S_5, and S_7) in the four-leg inverter, are either simultaneously at ON state (1111) or OFF state (0000). The resonant circuit operates at this moment to produce zero voltage across the inverter. The resonant operation cycle starts when

switch S_{3a} turned ON with zero current to build up the energy in the inductor[8]. The inductor current rises linearly, since S_{1a} and S_{2a} are at ON state, see Fig.4.

Mode-2 [t_1-t_2] At $t=t_1$ adequate energy of $(LI_P^2/2)$ is stored in the inductor. The switch S_{1a} turns OFF at this moment with zero voltage, because $V_{c1}=E$, this energy condition is necessary to ensure that V_{c1} and V_{c2} can return to E at the end of resonant cycle and preparing S_{1a} to turn ON again with zero voltage condition in the next operation of resonant circuit, as illustrated in Fig.4. When S_1 is OFF the inductor energy transfer, and discharge the capacitors C_1 and C_2 through S_{2a}, therefore the voltage across C_1 and C_2 resonant from +E to $-V_{c1max}$ and the inductor current will rise from the critical value I_p to peak current value I_{Lmax}, which affect the circuit operation. The inductor current and capacitors voltage can be calculated as follows:

$$I_L=(I_P + I_o)\cos\omega_1 t'+\frac{E}{z_o}\sin\omega_2 t'-I_o \quad (1)$$

$$V_{C1}(t)=V_{C2}(t) \quad (2)$$

$$V_{C2}(t)=-(I_P + I_o)z_o\cos\omega_1 t'+\frac{E}{z_o}\sin\omega_2 t'+ E\cos\omega_2 t' \quad (3)$$

where,

$$t'=t-t_1$$

$$C=C_1+C_2$$

$$\omega_1=\frac{1}{\sqrt{LC}}$$

$$z_o=\sqrt{\frac{L}{C}}$$

Mode-3 [t_2-t_3] The inductor current iL rise to its peak positive value iLmax, so, V_{c1} and V_{c2} are zero since diL/dt=0 at $t=t_2$. In addition, S_{2a} turned OFF with zero voltage, the PRDCL circuit then split into two parts, when the voltages V_{c1} and V_{c2} start to become negative, which is not desirable for the inverter operation. Therefore to clamp the negative voltage of V_{c2} to zero value, and for adequate time of zero voltage across the inverter when the zero space vector occurs, the switch S_r turns ON at $t=t_2$ since Io connected across the DC link. The first part of the PRDCL in this mode is resonant circuit (L-C1) and the second part is a clamp circuit (C_2 and S_r) which responsible for zero voltage across the device. The equations of the inductor current and the capacitors voltage are as follows:

$$I_L(t)=I_{Lmax}\cos\omega_2 t' \quad (4)$$

$$V_{C1}(t)=-V_{C1max}\sin\omega_2 t' \quad (5)$$

$$V_{C2}=0$$

where,

$$t'=t-t_2$$

$$\omega_2=\frac{1}{\sqrt{LC_1}}$$

$$V_{C1max}=\omega_2 LI_{Lmax} \quad (6)$$

Mode-4 [t_3-t_4] In this mode i_L attains the negative peak value $-i_{Lmax}$, V_{c1} changes its value from negative to zero, since $d_{iL}/dt = 0$ at $t=t_3$, then this voltage changes its direction, at that time S_{2a} and S_r must be at ON and OFF state respectively, to allow charging of C_1 and C_2 with the stored energy in the next period. The equations for inductor current and capacitors voltage are as follows:

$$I_L t=(I_o-I_{Lmax})\cos\omega_1 t'-I_o \quad (7)$$

$$V_{C1}(t)=V_{C2}(t)=(I_{Lmax}-I_o)z_o\sin\omega_1 t' \quad (8)$$

where,

$$t'=t-t_3$$

Mode-5[t_4-t_5] At $t=t_4$,V_{c1} and V_{c2} attains the voltage value of E while i_L equal to some negative value , S_{a1} is turned ON with zero voltage again, therefore i_L starts to increase linearly.

Mode-6 [t_5-t_0+T_s] At t= t_5, i_L returns to zero and the switch S_{a3} is turned OFF with zero current (natural commutation). After t_5, S_{a1} and S_{a2} are still ON, while S_3, and S_r, stay OFF until time t_o + T_s when another zero voltage across the inverter is requiered. This completes one switching cycle of the inverter resonant circuit. By some manipulations, several important design formulas can be derived as follows[8, 9]:

$$I_{Lmax}=\frac{E}{z_o}+I_o \quad (9)$$

$$V_{C1max}=\sqrt{\frac{L}{C_1}}\, I_{Lmax} \quad (10)$$

$$(t_2-t_1)=\frac{1}{\omega_1}\sin^{-1}\left(\frac{E}{E+2z_oI_o}\right) \quad (11)$$

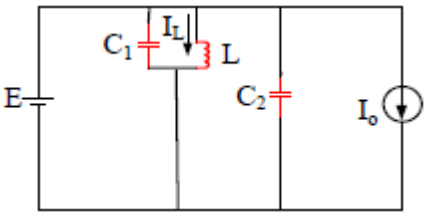
$$I_P=\frac{E}{z_o}\cot[\omega_1(t_2-t_1)]-I_o \quad (12)$$

$$(t_1-t_o)=\frac{L}{E}I_P \quad (13)$$

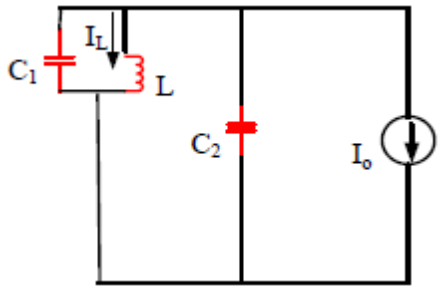
$$(t_3-t_2)=\frac{\pi}{\omega_2} \quad (14)$$

$$(t_4-t_3)=\frac{\pi}{2\omega_1} \quad (15)$$

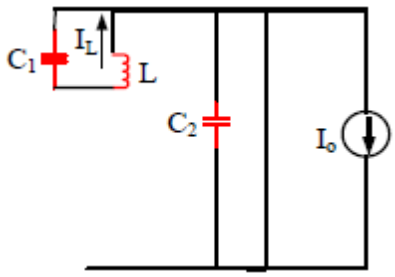
$$(t_5-t_4)=\frac{L}{E}I_o \quad (16)$$



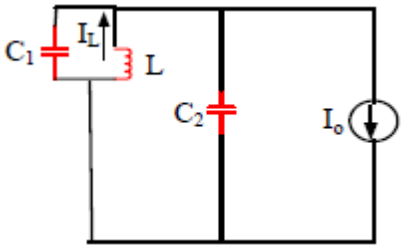
Mode-1



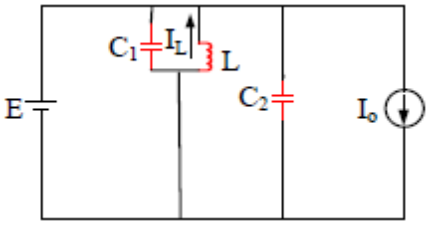
Mode-2



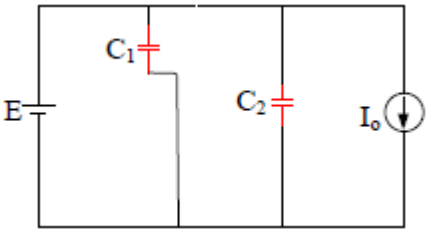
Mode-3



Mode-4



Mode-5



Mode-6

Fig.3 Resonant circuit modes of operation.

V. Inverter input current I_o

The SVPWM inverter modeled by a current source whose value changes as a step function during the resonant transition. Step changes in the inverter input current inevitably occurs under normal operating conditions[10]. By addressing the switching logic sequence and the inverter phase currents, the current I_o can be computed. Table-1 summarizes the relation between I_o with respect to the phase currents for different switching patterns of the inverter[11].

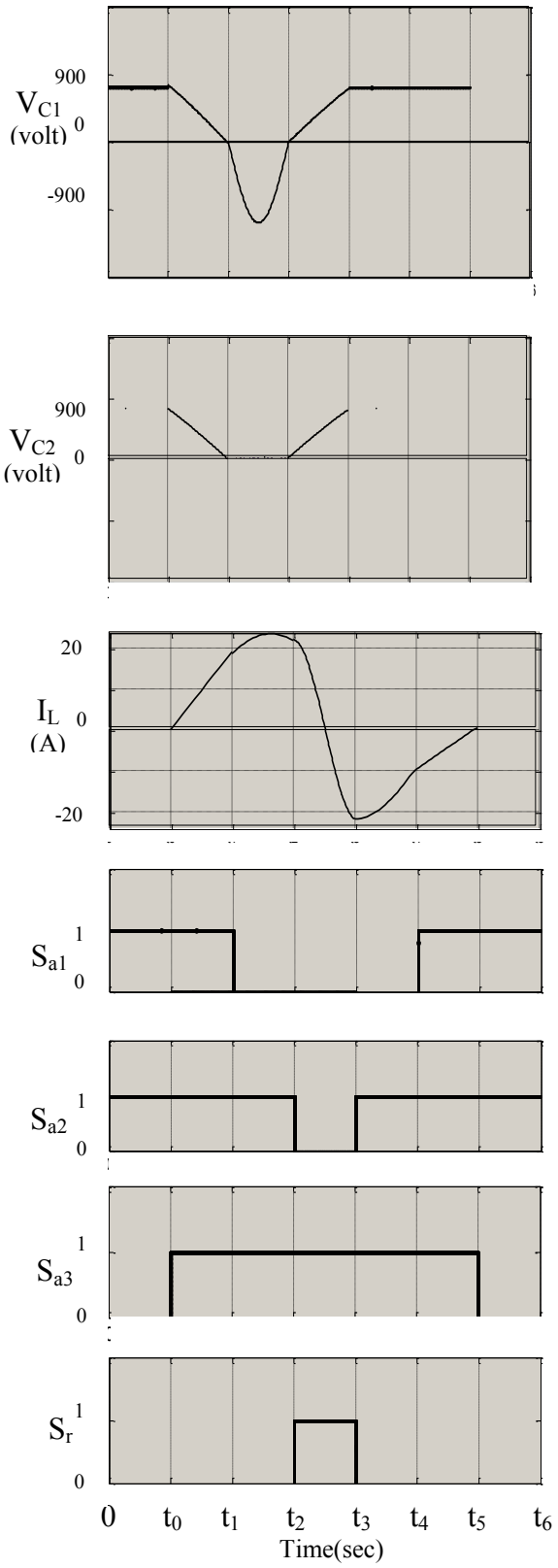


Fig.4 Resonant circuit waveforms.

Table-1 Inverter input current for different switching patterns.

Switching pattern	On-switches	Inverter input current
1	S_1, S_3, S_5	$i_a+i_b+i_c=0$
2	S_1, S_3, S_2	$-i_c$
3	S_1, S_6, S_5	$-i_b$
4	S_1, S_6, S_2	i_a
5	S_4, S_3, S_5	$i_b + i_c = -i_a$
6	S_4, S_3, S_2	i_b
7	S_4, S_6, S_5	$-i_a$
8	S_4, S_6, S_2	$0 (i_a + i_b + i_c) = 0$

The following simple relation derived by Boolean manipulation of Table-1.

$$I_o=S_1 i_a+S_3 i_b+S_5 i_c \quad (17)$$

VI. PRDCL Operation with Four-leg SVPWM Inverter

It is clear that the resonant circuit operation demands minimum period, to ensure a complete oscillation between its modes[3]. This operation imposes a condition, where the PWM cycle must be longer than the minimum pulse duration. Furthermore, the long periods needed for resonant cycle, leads to smaller modulation indices.

The four-leg space vector PWM inverter with, symmetrically aligned sequence used in this work, requires eight resonant cycles in every switching period Ts, which results in poor DC link voltage utilization and less range of switching frequencies. In four-leg SVPWM inverter the reference voltage vector obtained by:

$$|V_{ref}|e^{j\theta ref}.T_s=d_1.\overrightarrow{V_1}+d_2.\overrightarrow{V_2}+d_3.\overrightarrow{V_3} \quad (18)$$

and

$$d_0=1-d_1-d_2-d_3 \quad (19)$$

where, d_1, d_2, and d_3 are the duty ratios of the switching vectors. The zero-vector represented by the upper inverter switches V_0 (1111) or V_{15} (0000), appears twice in every switching cycle, this shown in Fig.5.

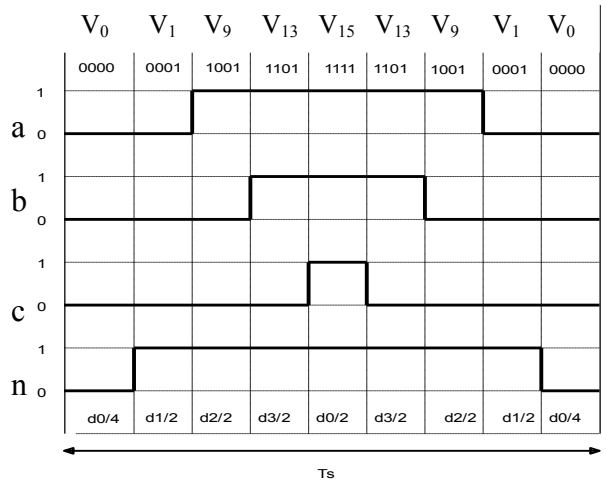


Fig.5 Symmetrically aligned sequence (pattern) for tetrahedron T_1.

In this work a modified modulation sequence used, zero-vector (V_0 or V_{15}) represents the zero voltage period (t_z) generated by the resonant circuit, therefore the modified SVPWM requires only two resonant cycles in each switching period Ts, as shown in Fig.6.

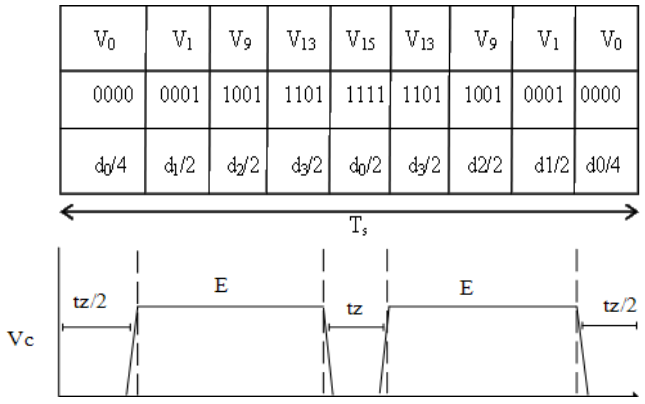


Fig.6 Modified SVPWM with zero voltage periods.

There are two main requirements have considered in the resonant circuit operating cycle when zero-vector occurs:

1-The resonant cycle must be completed prior to the next cycle.

2-The short duty ratios (less than the resonant zero voltage's period) have to be eliminated.

The load current and the resonant circuit components are the main factors affecting the width of each resonant cycle. Therefore, for maximum load current and given resonant circuit elements, the maximum time to complete one resonant cycle should be less than tz.

The parameters used for the theoretical and simulation studies are:

E=850V, I_L=20A, L=47.2µH, C_1=0.44µF, C_2=2nF, R_L=14.14Ω, L_{filter}=3.5mH, C_{filter}=400µF, switching frequency=5 kHz. SEMKRON (SKM50GAL12T4) IGBT selected as a switch, using its data, current (fall time, rise time, and tail time) in inverter model (IGBT block) and circuit design. The resonant circuit elements designed and selected like a regular turn ON and turn OFF snubber circuit[4]. The capacitor C can be calculated as:

$$C=\frac{I_o t_f}{2V_d}$$

where, I_o is the load current, V_d is the dc link voltage, and t_f is the IGBT current fall time.

The inductor L can be calculated as:

$$\Delta V_{CE}=\frac{LI_o}{t_r}$$

where, ΔV_{CE} is the transistor voltage drop during the turn-on state, t_r is the IGBT current rise time.

VII. Simulation of PRDCL Soft-switching Four-leg SVPWM Inverter

The Matlab/Simulink implemented model of the soft-switching four-leg inverter with PRDCL resonant circuit illustrated in Fig.7. Five main subsystems block contained in inverter subsystem block see Fig.8. The first block represents the SVPWM, which generates the conventional SVPWM pulses, the second block provides the sharp edge shaping of the switching signal, the inverter input current computed in the third block. The fourth block applies the soft switching, which detects the occur of zero-vector in each switching cycle, and thus activating the resonant circuit switches to produce zero voltage periods. The fifth block of the model represents the four-leg inverter with PRDCL resonant circuit.

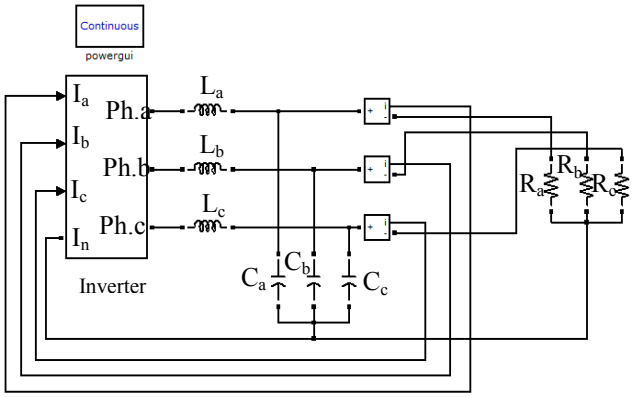


Fig.7 Implemented Matlab/Simulink model of the soft-switching four-leg inverter.

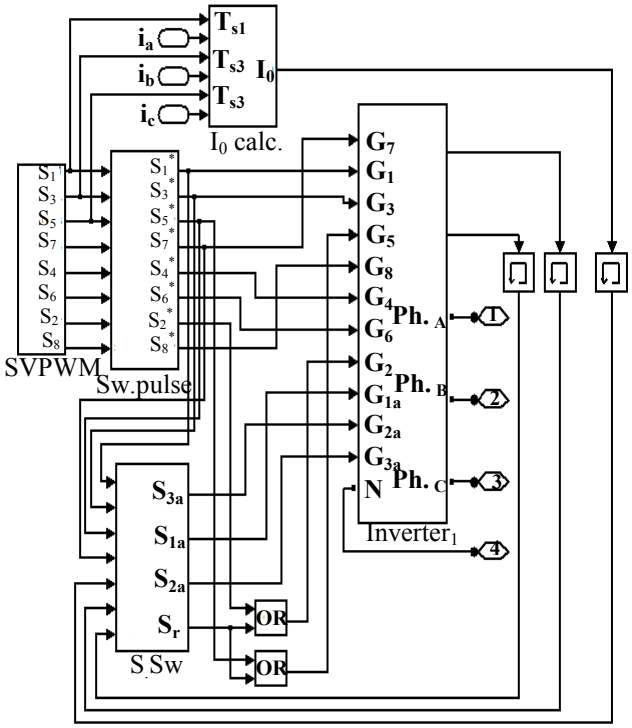


Fig.8 Subsystems contained in inverter subsystem block.

The internal construction of switch pulse block contains relational operator blocks for shaping the edges of switching pulses for accurate timing. This is shown in Fig.9. The third block is (I_o computing) which is responsible for predicting and computing inverter input current necessary to control resonant circuit using Table-1 and Eq.17. In addition, average input DC power is computed in this block, see Fig.10.

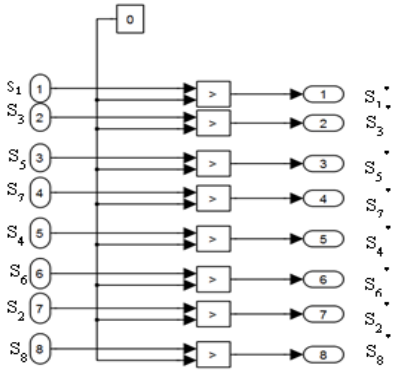


Fig.9 Inner diagram of (switch pulse) block.

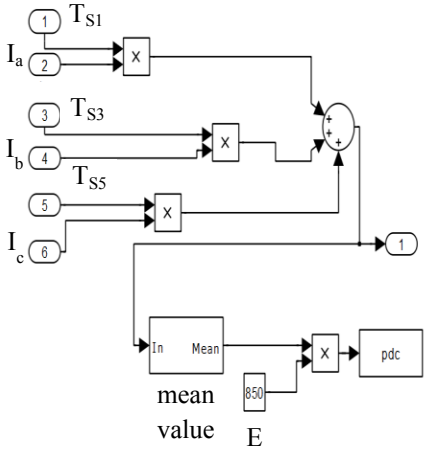


Fig.10 Inner diagram of (I_0 calc.) block.

The fourth block is the (soft-switching), in this block many logic blocks are used to detect the occurrence of zero-vector (1111 or 0000) in each switching cycle to activate the resonant circuit switches, also controlling the (ON / OFF) period for each switch. Figure 11 shows the details of this block. Inside this block there is (resonant cycle timing) block, which receives inverter input current, capacitor voltage, and inductor current as input signals, then computing critical inductor current value (I_P) for successful resonant circuit operation, also the different time periods and maximum inductor current are computed in this block. These values are used to generate the required switching commands (ON or OFF) to control the resonant circuit operation and hence the exact timing to each modes of

operation in each dependent cycle. The detail construction of this block is shown in Fig.12.

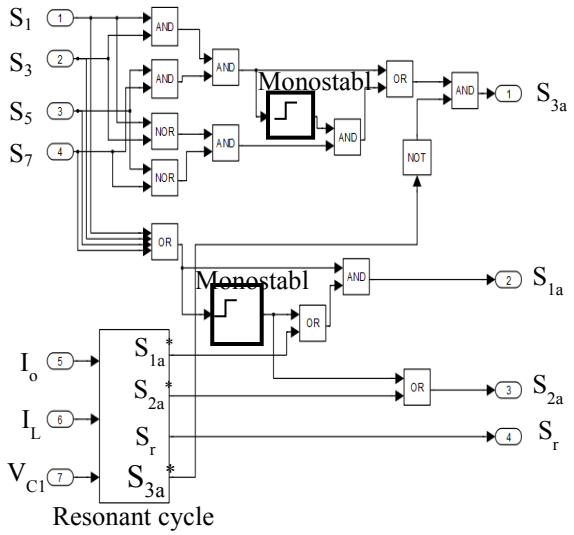


Fig.11 Inner diagram of (soft-switching) block**.**

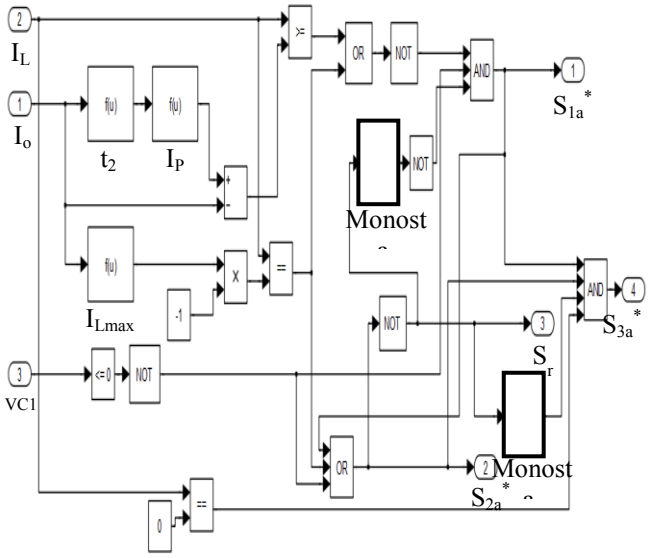


Fig.12 Detail diagram for (resonant cycle timing) block.

The last block (inverter1) contains the inverter switches and resonant circuit elements, IGBT blocks are used, and its parameters selected according to manufacturer data sheet. The inverter internal block and its connections are shown in Fig.13.

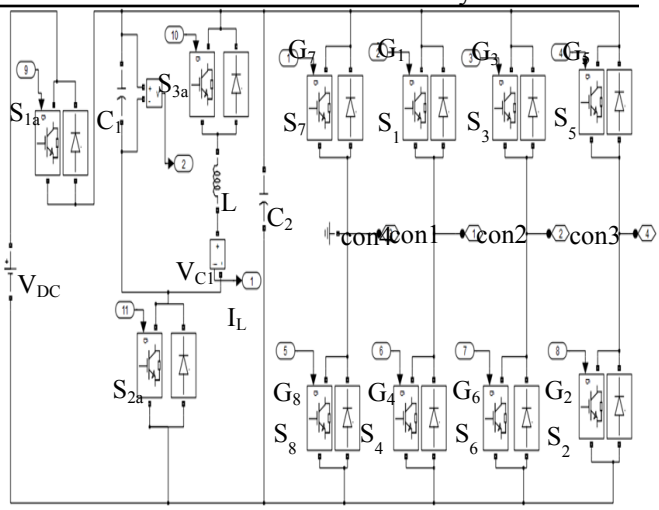


Fig.13 Four-leg inverter block with PRDCL resonant circuit.

VIII. Simulation Results

Matlab/Simulink program is used to simulate PRDCL four-leg inverter. The selection process of the resonant circuit components parameters, based on the design formulas and the necessary considerations, which discussed in the previous section. Both balanced and unbalanced inverter loads used to confirm the resonant circuit results. Figures (14-16) show the three-phase inverter output voltages, load currents, and neutral current for balanced load. These figures show that the main features of the four-leg inverter are fulfilled when the PRDCL circuit is added to the inverter. The four-leg inverter switches (S_1, S_3, S_5, and S_7) firing pulse with capacitor voltage V_{C2}, shown in Fig.17. During zero-vector (1111 or 0000) occurrence, the capacitor voltage value is zero. This verifies the simultaneous operation of the resonant circuit with zero-vector occurrence. The resonant circuit switches (S_{a1}, S_{a2}, S_{a3}, and S_r) sequences of operation with DC-link capacitor voltage V_{C2}, shown in Fig.18, which confirm with the resonant circuit analysis, see Fig.4. The resonant circuit principle of operation states that, the maximum inductor current occurs when capacitor voltage is zero and vice versa. This is clearly shown in Fig.19.

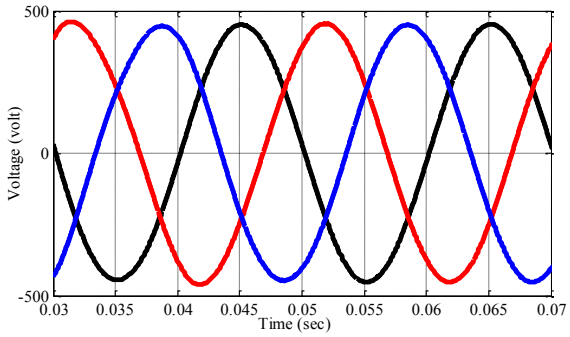


Fig.14 Inverter three-phase output voltages (balanced load).

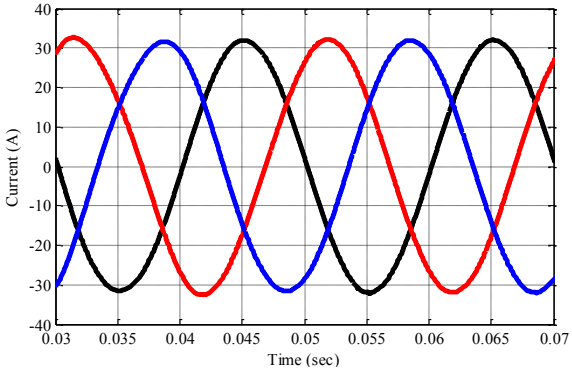


Fig.15 Inverter three-phase output load currents (balanced load).

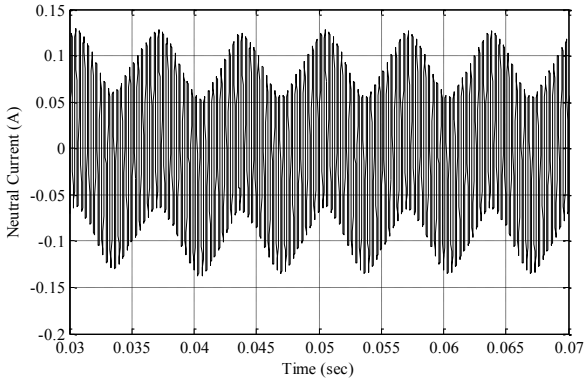


Fig.16 Inverter output neutral current (balanced load).

Figures 20-23 show currents and voltages for different switches with DC-link capacitor voltage V_{C2}, one can note that switches are ON with zero voltage due to resonant circuit operation, this occurs when these switches are involved with zero-vector, while the resonant circuit is inactive when active vector are in action.

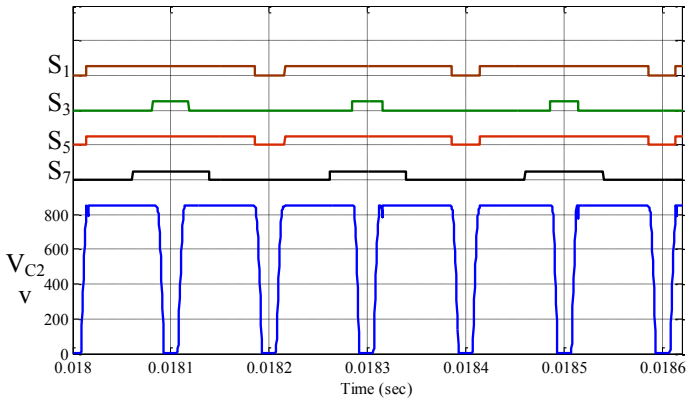


Fig.17 Inverter upper switches pulse with DC-link capacitor voltage.

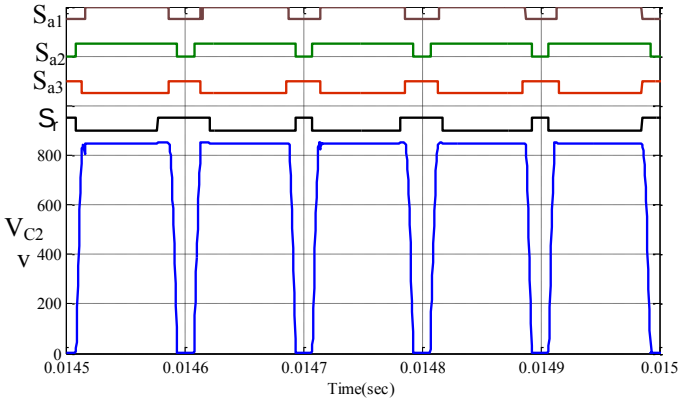


Fig.18 Resonant circuit switches pulse with DC-link capacitor voltage.

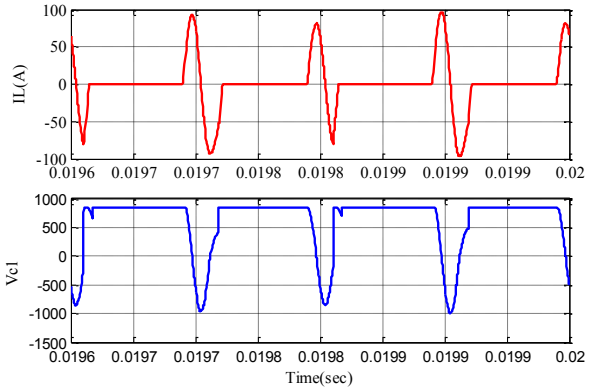


Fig.19 Resonant circuit inductor current and capacitor voltage.

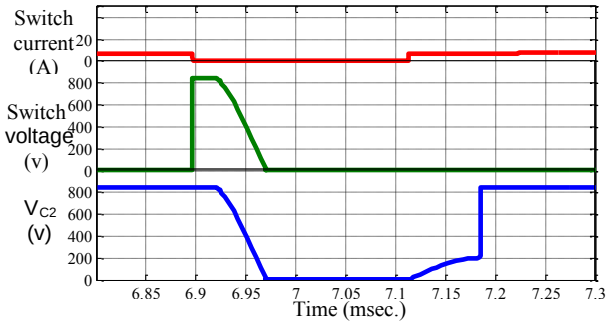


Fig.20 Switch S_1 current and voltage with V_{C2} during switch ON transition.

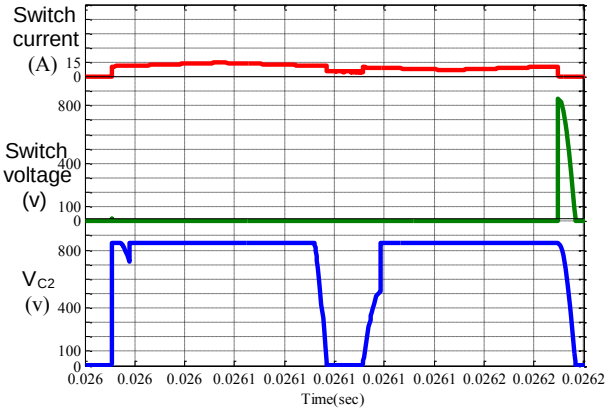


Fig.21 Switch S_1 current and voltage with V_{C2} when the switch deals with active vector.

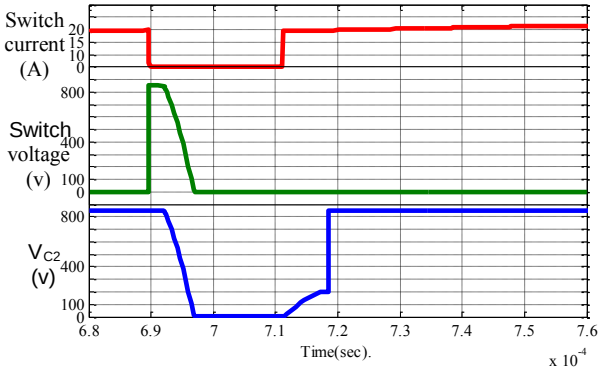


Fig.22 Switch S_6 current and voltage with V_{C2} during switch ON transition.

The inverter input current Io shown in Fig.24. This current affects the length of each dependent resonant cycle as discussed earlier.

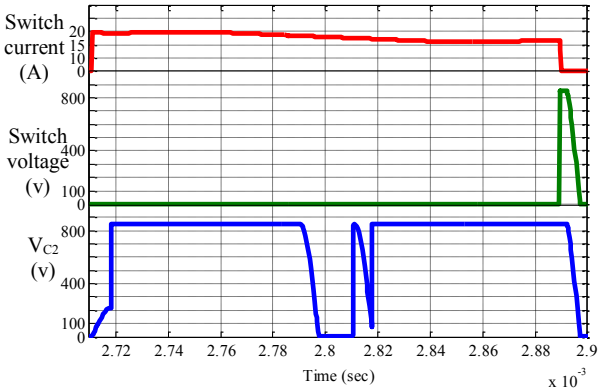


Fig.23 Switch S_1 current and voltage with V_{C2} when the switch deals with active vector.

The mean switching losses in S_1 (as an example) for hard, and soft switching is shown in Fig.25, this figure verify the effectiveness of the proposed utilization of the PRDCL circuit with SVPWM four-leg inverter in reducing the switching losses about (30%). The inverter input power for hard and soft switching with balanced load condition shown in Fig.26. This figure confirms the reduction of the switching losses when the PRDCL resonant circuit used. The THD of the output voltage calculated for both cases hard and soft switching shown in Fig.27, the two results are identical, since the resonant circuit operation not affect the THD. This is due to the simultaneous operation of the resonant circuit with zero-vector periods. The Simulation repeated for unbalanced load to verify the results obtained earlier. The results prove that the main features of four-leg SVPWM inverter maintained.

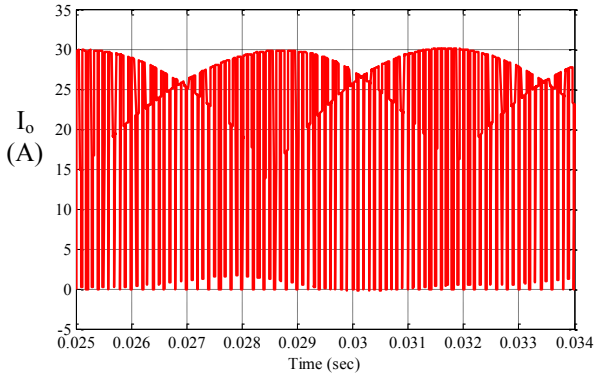


Fig.24 Inverter input current I_0.

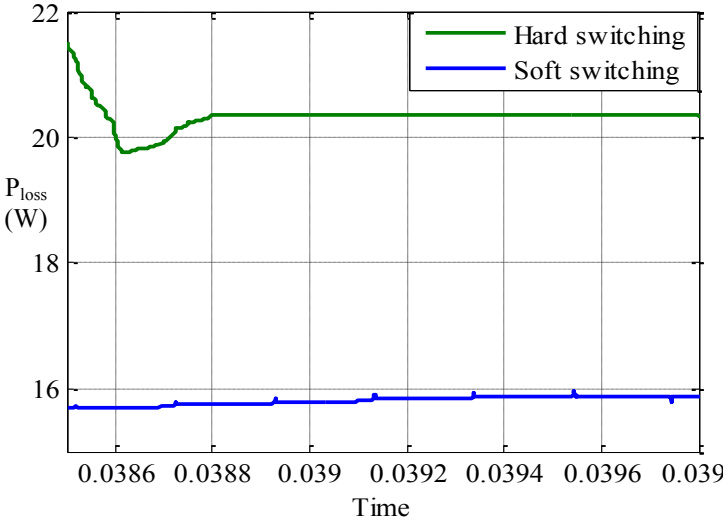


Fig.25 Mean switching losses for S_1 (hard, and soft switching).

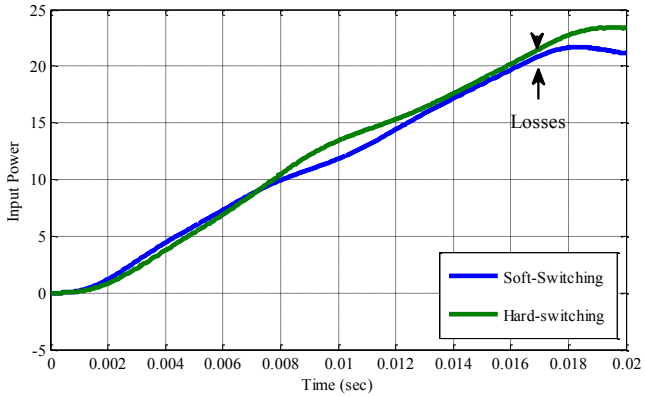


Fig.26 Inverter input power for hard, and soft switching with balanced load condition.

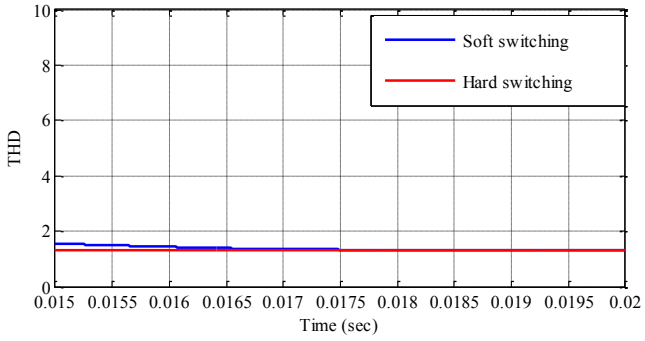


Fig.27 Inverter output voltage THD for hard, and soft switching.

The three-phase inverter output voltages, load currents, and neutral current for unbalanced load shown in Figs.28 and 29. In spite of unbalanced load currents and neutral current, the output voltages still balanced. The currents and voltages for different switches with DC-link capacitor voltage V_{C2} are shown in Figs. 30 and 31, one can note that switches are ON with zero voltage due to operation of resonant circuit, this occurs when these switches are involved with zero-vector. The inverter input power for hard switching and soft switching with unbalanced load condition shown in Fig. 32. This figure confirms the reduction of the switching losses when the PRDCL resonant circuit is used.

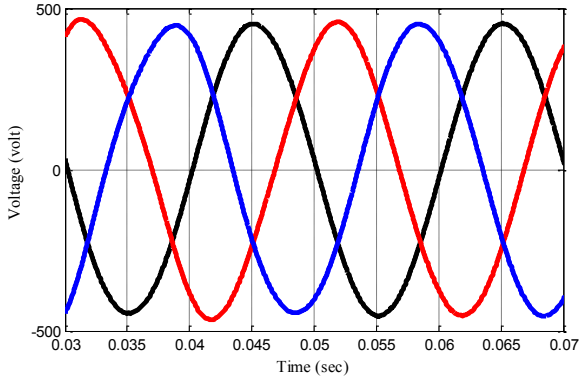


Fig.28 Inverter three-phase output voltages (unbalanced load).

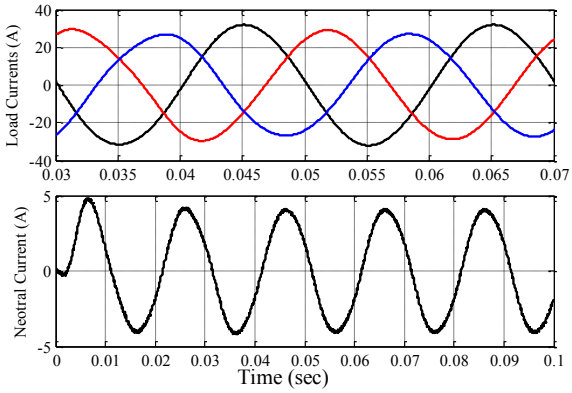


Fig.29 Inverter three-phase output load currents (unbalanced load).

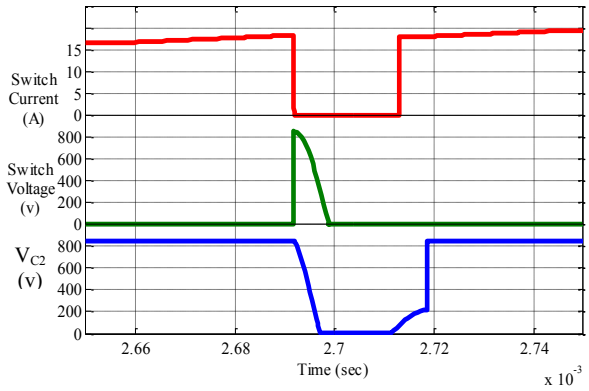


Fig.30 Switch S_1 current and voltage with V_{C2} during switch ON transition.

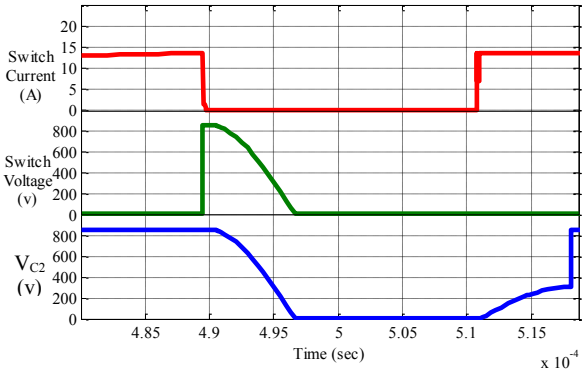


Fig.31 Switch S_6 current and voltage with V_{C2} during switch ON transition.

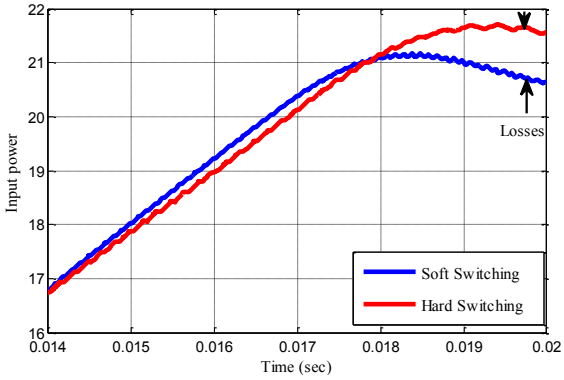


Fig.32 Inverter input power for hard, and soft switching with unbalanced load condition.

IX. CONCLUSION

In this paper a Matlab/Simulink model of the proposed three-phase four-leg SVPWM inverter with PRDCL resonant circuit presented. The PRDCL circuit connected between the high-voltage DC source and the inverter. The resonant circuit activated only during the zero-vectors period, which results in a zero-voltage across the inverter switches. This action provides a short period of zero-voltage condition to the switches involved during the transition between the zero and active vectors. The resonant circuit switches sequence of operation is accurately designed according to the circuit parameters and load conditions. SVPWM with symmetrically aligned technique is used to compare the hard and soft switching operation.

It is possible to present the superiority in total power loss characteristic of the soft switching inverter from that of hard switching inverter. The inverter output voltage THD remains unchanged in soft switching, since operation of the resonant circuit is in zero-voltage period.

Two load conditions (balanced and unbalanced) were investigated simulation results in both cases confirm the effectiveness of the proposed soft-switching four-leg SVPWM inverter circuit. Successful operation of the circuit demonstrated in simulation implementation.

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