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Coding-Decoding Ternary Logic

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Abstract

In this paper ternary logic is encoded into binary and certain processes were conducted on binary logic after which the binary is decoded to ternary. General purpose digital devices were used and the circuit is designed back to front starting from ternary logic provided by transistor pairs at output side back to front end. This provided easier design technique in this particular paper. Practical and simulation results are recorded.

Keywords: Logic, ternary- binary conversion, coding, decoding.

تشفير المنطق الثلاثي

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الخلاصة

في هذا البحث يتم تشفير المنطق الثلاثي الى ثنائي ويتم اجراء بعض العمليات على المنطق الثنائي التي يتم بعدها الاعادة الى الشفرة الثلاثية. استخدمت النبائط الرقمية للاغراض العامة(general purpose devices) في تصميم الدائرة الذي يتم من مرحلة الاخراج (output) الى مرحلة الادخال (input) بدءا من المنطق الثلاثي باستخدام ازواج الترانزستور في جهة الاخراج والعودة الى جهة الادخال. هذا يجعل تقنية التصميم اسهل (في هذا البحث خاصة). ولقد تم تسجيل النتائج العملية ونتائج المحاكاة للدائرة العملية.

1. Introduction

Three valued, or ternary, logic[1] offers several important advantages over binary logic in the design of digital systems. For example[1-5] more information can be transmitted over a given set of lines or stored for a given register length, the complexity of interconnections can be reduced, deduction in chip area can be achieved, and more efficient error detection and correction codes can be employed. Furthermore, serial and some serial-parallel arithmetic operations can be carried out at higher speeds. To[6] interface a balanced ternary arithmetic unit with the external world, we must devise procedures for conversion of numbers to/from balanced ternary from/to decimal or binary format.

The Multiple-Valued Logic (MVL) [5,7] is implemented in two modes i.e. current mode and voltage mode. In the current mode operation, MVL states are defined in terms of output current, which is an integral multiple of reference current, and in voltage mode, MVL states are in terms of distinct voltage levels. This work is based on the latter mode, where three levels of voltages (5, 2.5, and 0) are used to represent ternary trits (2, 1, and 0) respectively. The designed system includes converting ternary logic to binary and vice versa.

Ternary and quaternary circuits[3] have been studied increasingly in recent years. Quaternary circuits have the practical advantage that a four-valued signal can easily be transformed into two-valued signal. However based on the following considerations, ternary circuits may be of more theoretical significance than quaternary:

a) Since 3 is the smallest radix higher than binary, ternary functions and circuits have the simpler form and construction. They can be studied and discussed easily yet they still display the characteristics of multivalued elements.
b) As a measure of the cost or complexity of multivalued circuits, the product of the radix and the number of signals has been proposed. Since 3 is the digit nearest to e=2.718, ternary circuits will be more economical according to this measure.
c) If balanced ternary logic (1, 0, -1) is used, the same hardware may be used for addition and for subtraction.
d) Since 3 is not integral power of 2, research on ternary logic may disclose design techniques that are overlooked in the study of binary or quaternary logic.

2. Preliminaries of Ternary Logic

The 20th century brought the extension to classical two-valued logic called n-valued logic for n>2. The most popular in the literature are three-valued logic, the finite-valued with more than three values and the infinite-valued (eg. Fuzzy logic) logics[2].

One of the main advantages of ternary logic[2,5]is that it reduces the number of required computation steps. Since each signal can have three distinct values, the number of digits required in the ternary family is $\log_3 2$ times less than that required in binary logic. It is assumed that ternary-logic elements can operate at speed approaching that of the corresponding binary logic elements.

In 1964, Alexander[2] showed that natural base (e=2.71828) is the most efficient base for implementation of switching circuits, where e is called Euler constant. Similarly e^2=7.38906 is more advantageous and most often used base in electronic computers with digits 0 and 1. The base e^3=20.0855 is more efficient.

Expanding the existing logic levels[2] to ternary and higher levels, higher processing rates could be achieved in various applications like memory management, communication throughput and domain specific computation. An evident advantage of a ternary representation over binary is economy of digits. To represent a number in binary system, one needs 58% more digits than that of ternary. Ternary representation admits sign convention also. This is the reason why ternary is casting its applications in the field of Fuzzy Logic, Machine Learning, Artificial Intelligence,…,etc.

There are two ways to represent ternary truth table:

i. Balanced ternary (BT) as in table-1.
ii. Ordinary ternary (OT) as in table-2.

Table-1 : Balanced Ternary logic

DEC	C	B	A
-13	-1	-1	-1
-12	-1	-1	0
-11	-1	-1	1
-10	-1	0	-1
-9	-1	0	0
-8	-1	0	1
-7	-1	1	-1
-6	-1	1	0
-5	-1	1	1
-4	0	-1	-1
-3	0	-1	0
-2	0	-1	1
-1	0	0	-1
0	0	0	0
1	0	0	1
2	0	1	-1
3	0	1	0
4	0	1	1
5	1	-1	-1
6	1	-1	0
7	1	-1	1
8	1	0	-1
9	1	0	0
10	1	0	1
11	1	1	-1
12	1	1	0
13	1	1	1

Table-2 Ordinary ternary Logic

DEC	C	B	A
0	0	0	0
1	0	0	1
2	0	0	2
3	0	1	0
4	0	1	1
5	0	1	2
6	0	2	0
7	0	2	1
8	0	2	2
9	1	0	0
10	1	0	1
11	1	0	2
12	1	1	0
13	1	1	1
14	1	1	2
15	1	2	0
16	1	2	1
17	1	2	2
18	2	0	0
19	2	0	1
20	2	0	2
21	2	1	0
22	2	1	1
23	2	1	2
24	2	2	0
25	2	2	1
26	2	2	2

3. Theoretical circuit

The circuit of this research involves encoding ternary logic to binary at the input side and vice versa at the output side with internal process between both sides as shown in block diagram of Fig.1.

Inputs are symbolized as S0S1S2 which may take (0, 2.5, or 5) volts. Each of these levels of voltages is encoded at the first stage of the system to a combination of BA (binary) as in table-3 by means of comparators.

Table -3: Ternary to binary encoder

Sos1s2	A	B
0	0	0
1	1	0
2	1	1

In the second stage, binary processes are achieved using S-R flip flops and logical gates as will be explained later.

The final (third) stage requires decoding the binary output of the binary processes in stage-2 to ternary logic as in table-4.

Table-4:Binary to ternary decoder

Q_A	Q_B	Q	Q'	Q"
0	0	0	1	2
1	0	1	2	0
0	1	2	0	1

This operation is implemented using switching circuits constructed by means of general purpose transistors with suitable bias, so that the transistors can operate at three states; saturation, cut off, and active regions (in between).

On operating under these conditions, transistors will give three output levels which simulates ternary logic.

4. Practical Circuit

The practical electronic circuit of the research system is shown in Fig.2. The design of the circuit started from the output stage (the decoder) which is constructed using two transistors as in Fig.3. So, to have three outputs (namely Q,Q',Q"), three pairs of transistors should be used for which the truth table is given by table-5.

Table-5: Truth table of stage three

A_1	A_2	B_1	B_2	C_1	C_2	Q	Q'	Q''
1	1	0	1	0	0	0	1	2
0	1	0	0	1	1	1	2	0
0	0	1	1	0	1	2	0	1

To generate the required logics on the bases of the transistors, S-R flip flops with Q_A and Q_B outputs are used (this is the second stage of the system).

All biases are expressed in terms of Q_A and Q_B as follows:

$$A_1 = \overline{Q_A}\ \overline{Q_B}\ ; \quad A_2 = \overline{Q_B}\ ;$$

$$B_1 = \overline{Q_A} Q_B\ ; \quad B_2 = \overline{Q_A}\ ;$$

$$C_1 = Q_A \overline{Q_B}\ ; \quad C_2 = Q_A \oplus Q_B$$

Table-6 shows the truth table of S-R flip flops where S_A and R_A are the inputs of flip flop A with output Q_A, and S_B and R_B are inputs of flip flop B with output Q_B.

Table-6: truth table of S-R flip flop

A	B	S_A	R_A	S_B	R_B	Q_A	Q_B
0	0	0	1	0	1	0	0
1	0	1	0	0	1	1	0
1	1	0	1	1	0	0	1

The first stage of the system requires encoding ternary logic ($S_0S_1S_2$) to binary (BA) as in table-3 (previously). Thus, inputs for S-R flip flops must be designed in terms of A and B. The following expressions are obtained using Boolean algebra according to table-6.

$$S_A = A\bar{B}\ ; \quad R_A = \bar{A}\bar{B} + \bar{A}B$$

$$S_B = \bar{A}B; \quad R_B = \bar{B}$$

Comparators are used in the first stage to convert ternary logic to binary as in Fig.4, for which it implements truth table-1.

5. Practical Results

Practical results taken at different stages of the circuit are recorded as in table.7 below. Fig.2 shows the simulation results of the state $S_oS_1S_2$ is logic 1 (2.5v).

6. Conclusion

Ternary code is more efficient than binary. Ternary logic is applied indirectly in the sense of using binary devices (transistors, CMOS,….etc.) oriented towards ternary code. This paper is one of such indirect mean which uses binary devices to effect ternary logic principles.

The practical circuit was designed by a method of back to front. That is starting to design final pair of transistors to obtain the ternary logic, then going back to design stage by stage down to front end of the circuit.

The circuit as a whole may be programmed on a microcontroller chip such as PIC16F84a or the like utilizing flow code or Xilinx methodology general purpose PLDs can also be used. In case of

PLDs: ABEL, VHDL or Verilog techniques can be applied to program the circuit on such PLDs. Such work is apt to be achieved next step as an anticipated ambition. Simulation results ensures the proper design for all three levels of input (ternary logic).

7. References

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Table-7: Practical results of the circuit

$S_0S_1S_2$	A	B	S_A	R_A	S_B	R_B	Q_A	Q_B	A_1	A_2	B_1	B_2	C_1	C_2	Q	Q'	Q''
0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	0	1	2
1	1	0	1	0	0	1	1	0	0	1	0	0	1	1	1	2	0
2	1	1	0	1	1	0	0	1	0	0	1	1	0	1	2	0	1

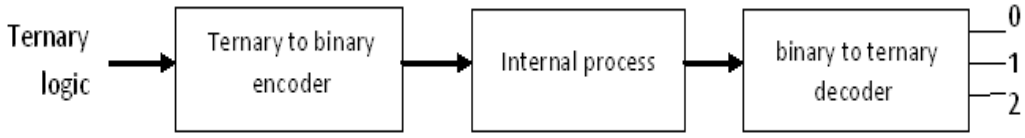

Fig.1: Block diagram of the circuit

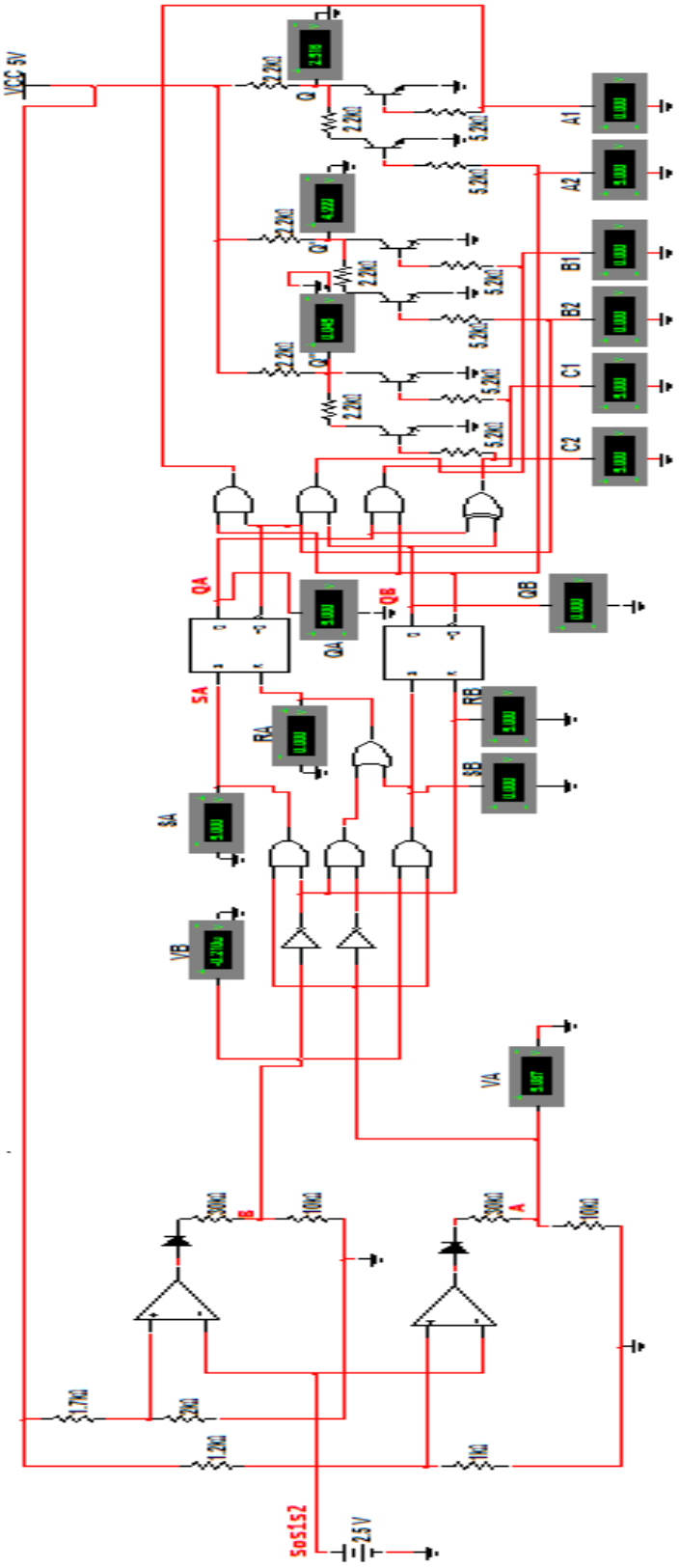

Fig.2 The practical electronic circuit

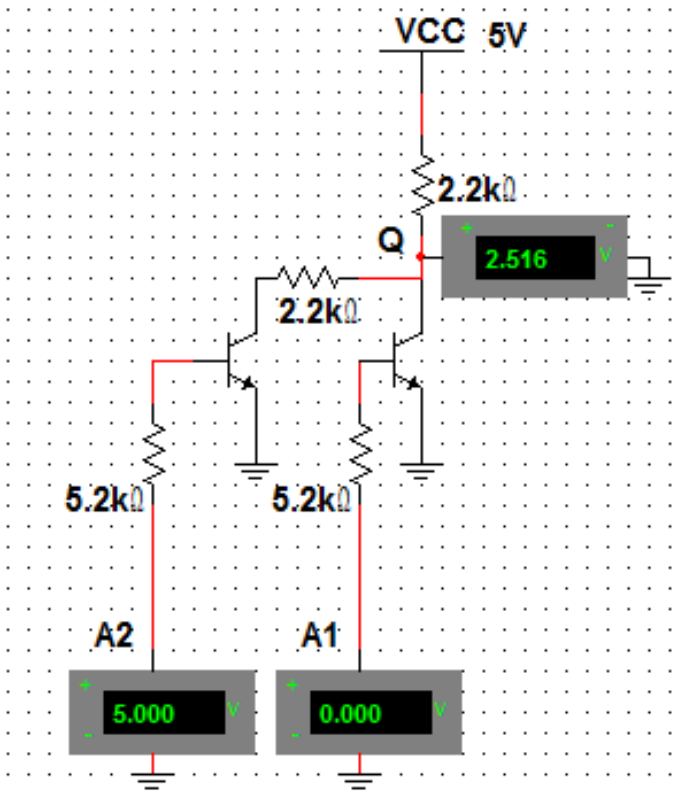

Fig.3 Two transistors constructing the decoder

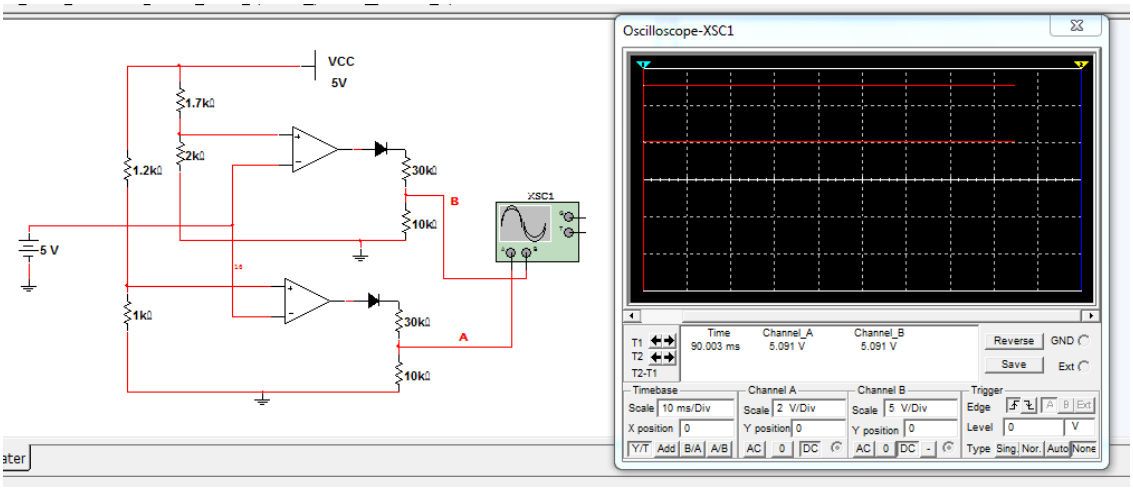

Fig.4 Comparators constructing the encoder.